



# Compal Confidential

## KAYF0 M/B Schematics Document

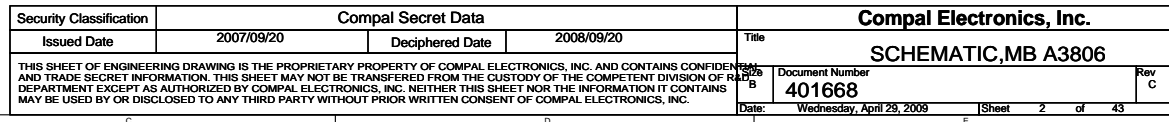
Intel Penryn Processor with Cantiga + DDRIII + ICH9M

2009-03-09

REV:1.0

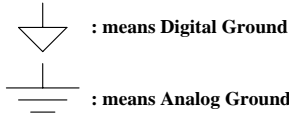
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**Model Name : KAYF0**  
**File Name : LA-5021P**



<div>power plane</div> <div>State</div>	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE  +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :



@ : means just reserve , no build  
DEBUG@ : means just reserve for debug.

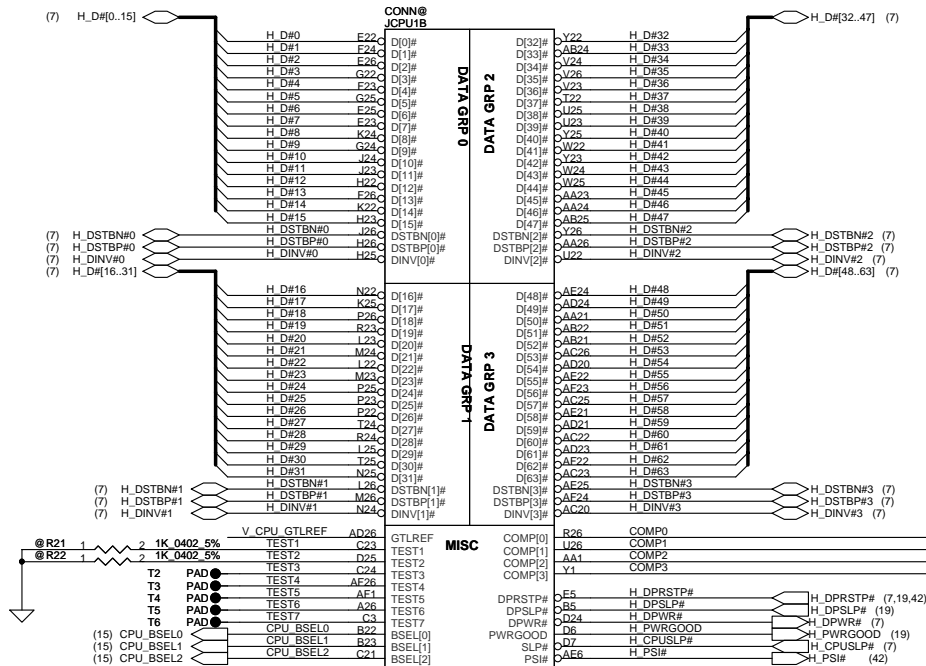
SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

I2C / SMBUS ADDRESSING

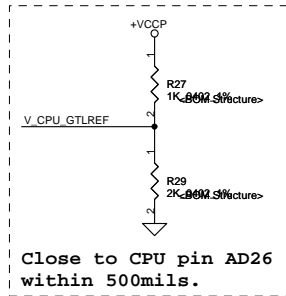
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0



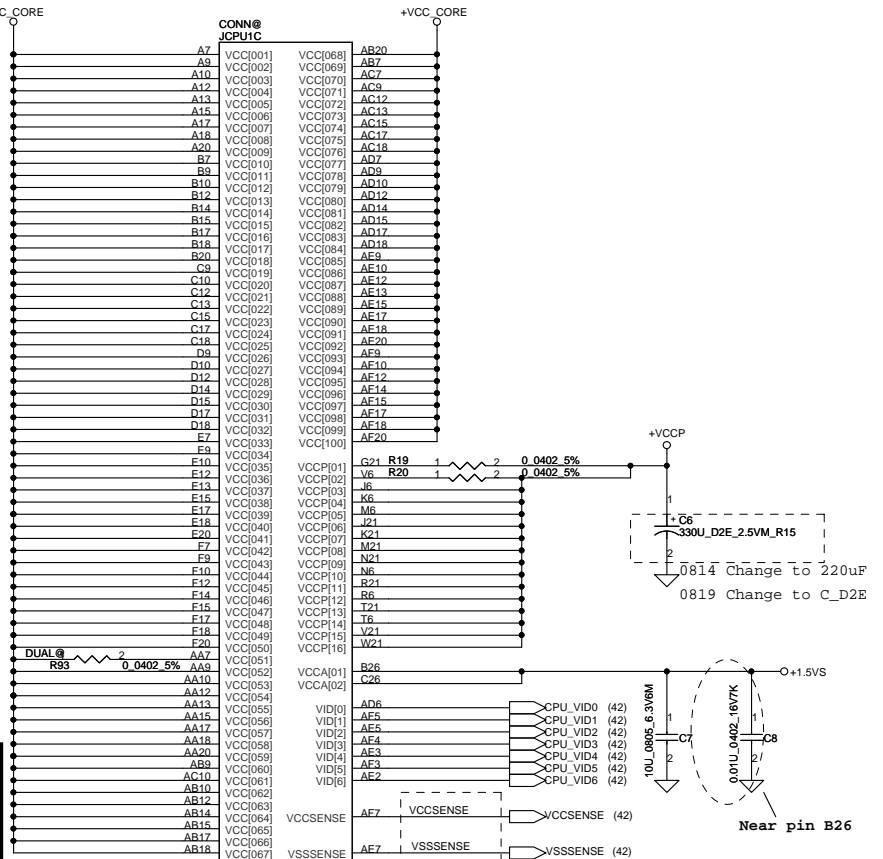


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

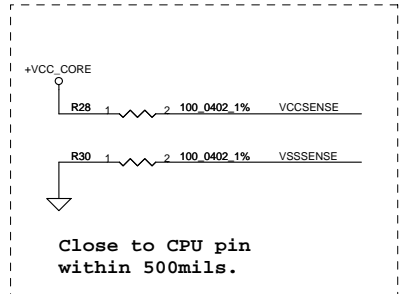
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

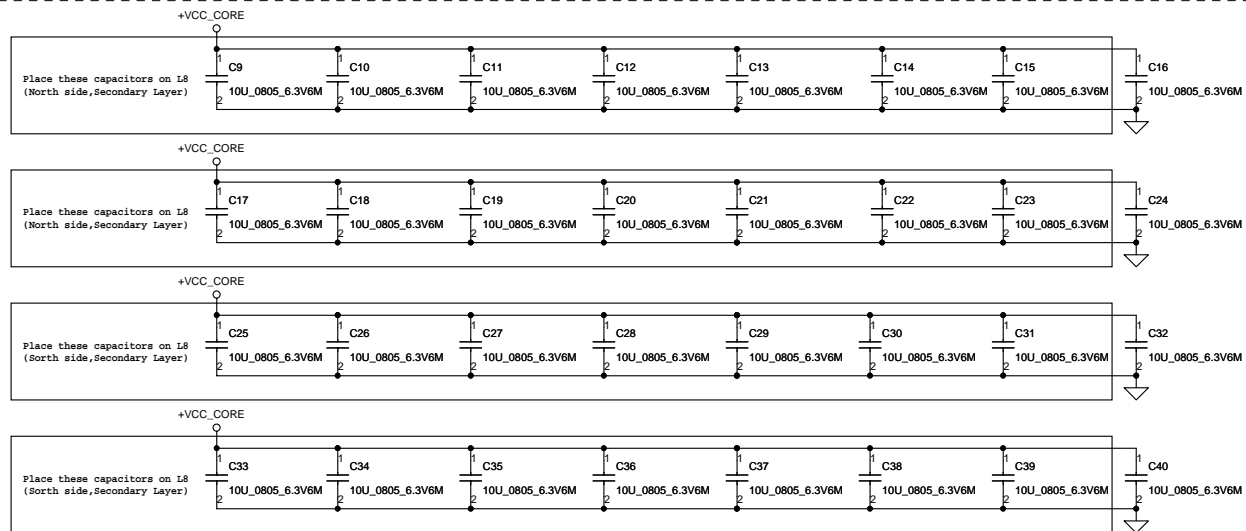
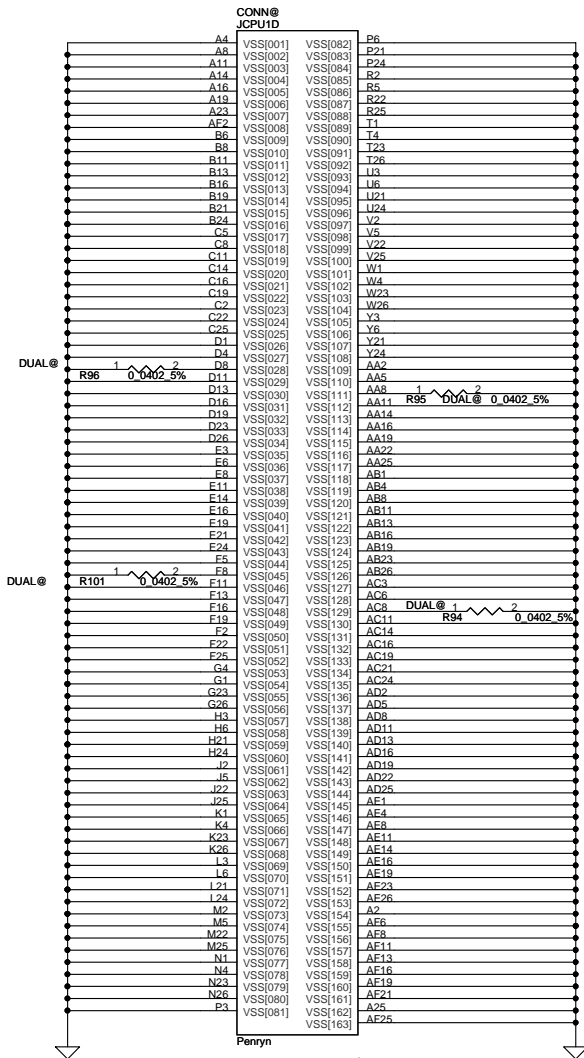


Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

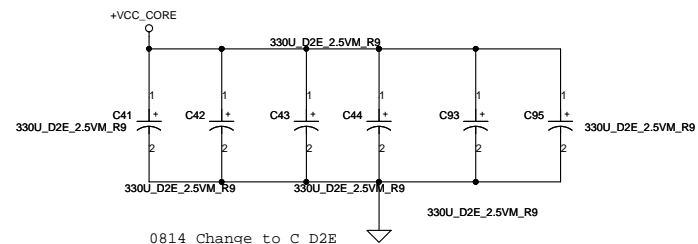


Length match within 25 mils. The trace width/space/other is 20/7/25.

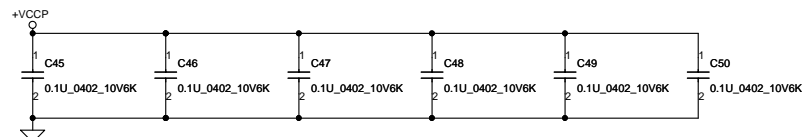




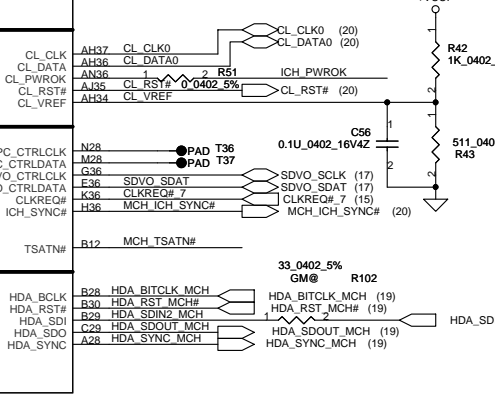
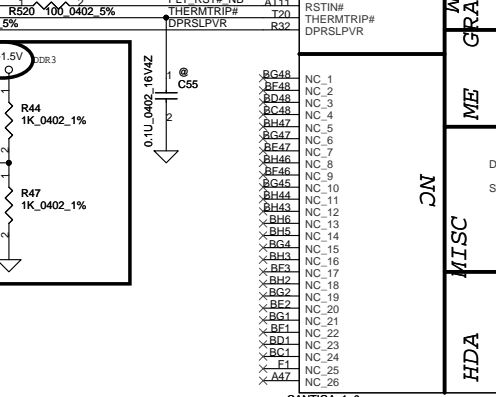
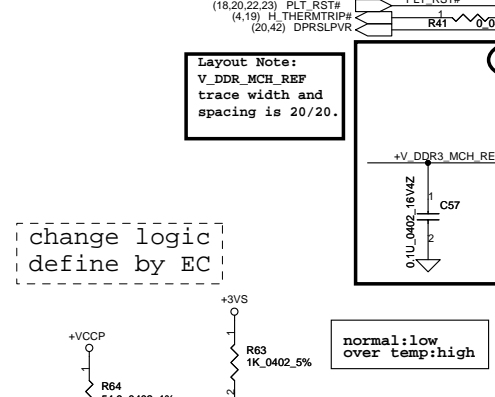
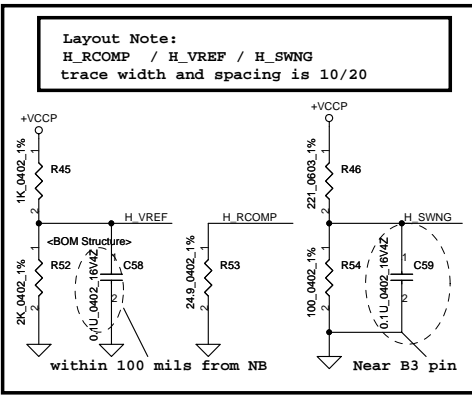
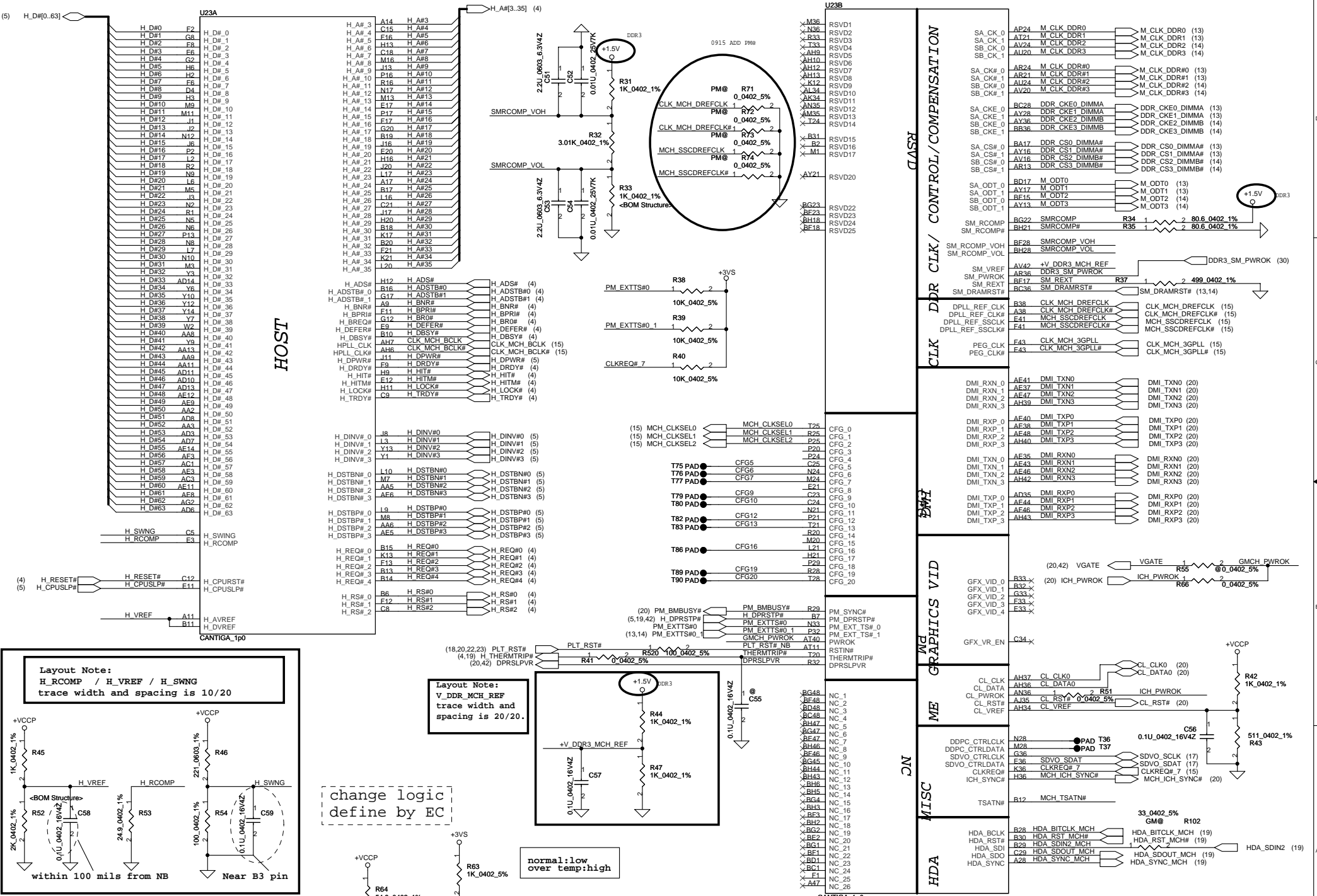
### Mid Frequency Decoupling



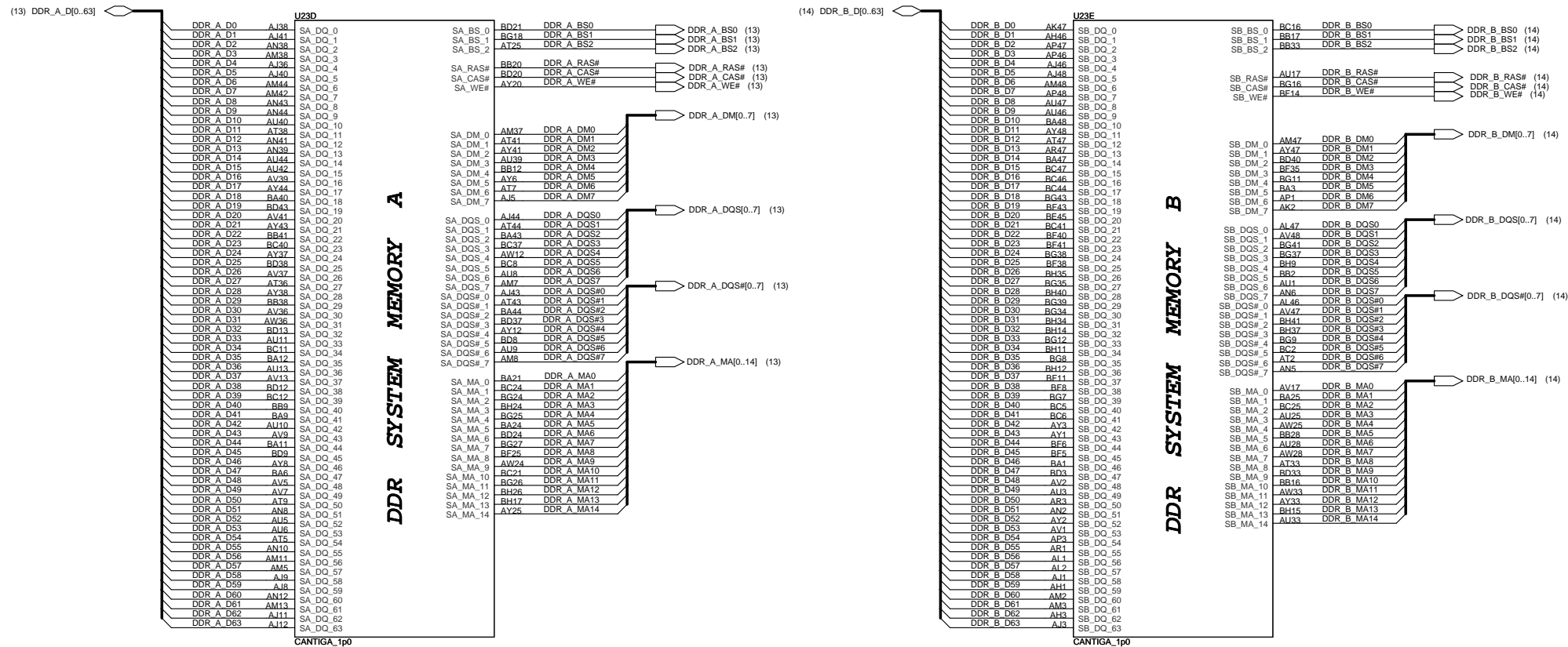
Place these inside socket cavity on L8 (North side Secondary)



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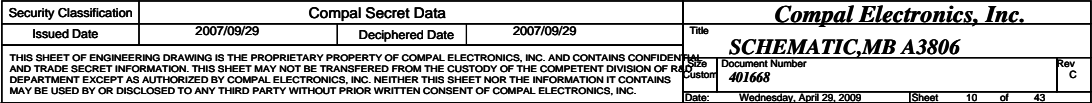
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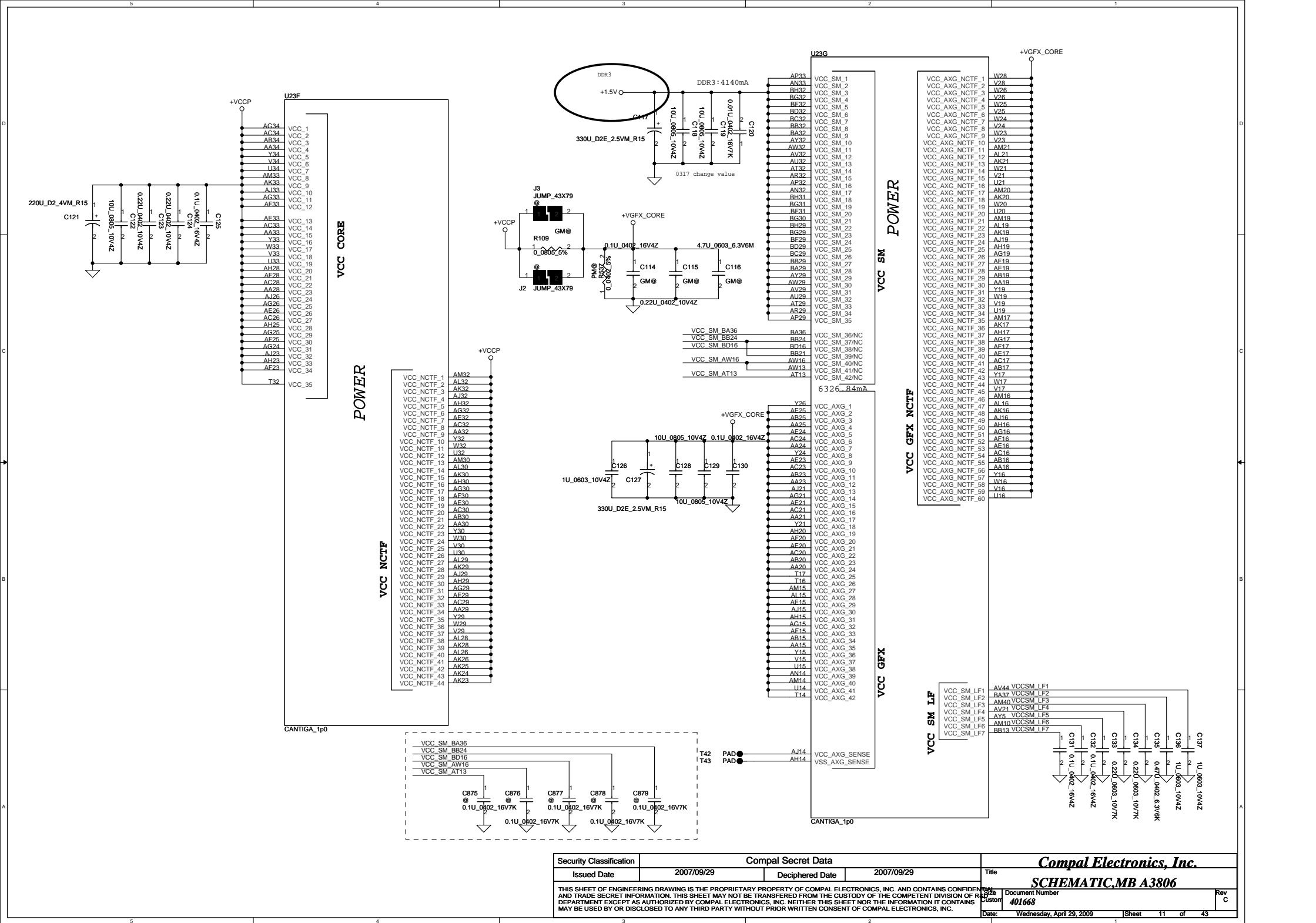


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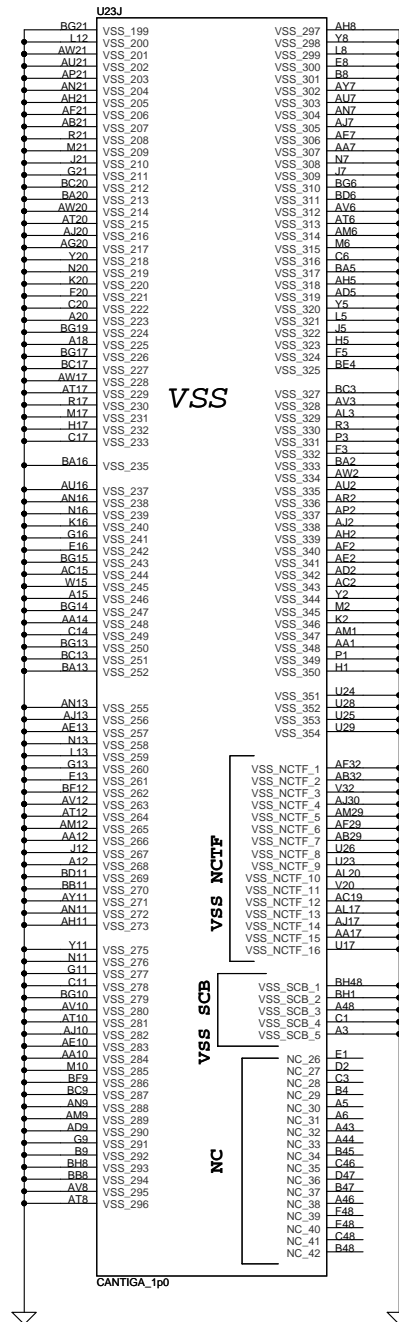
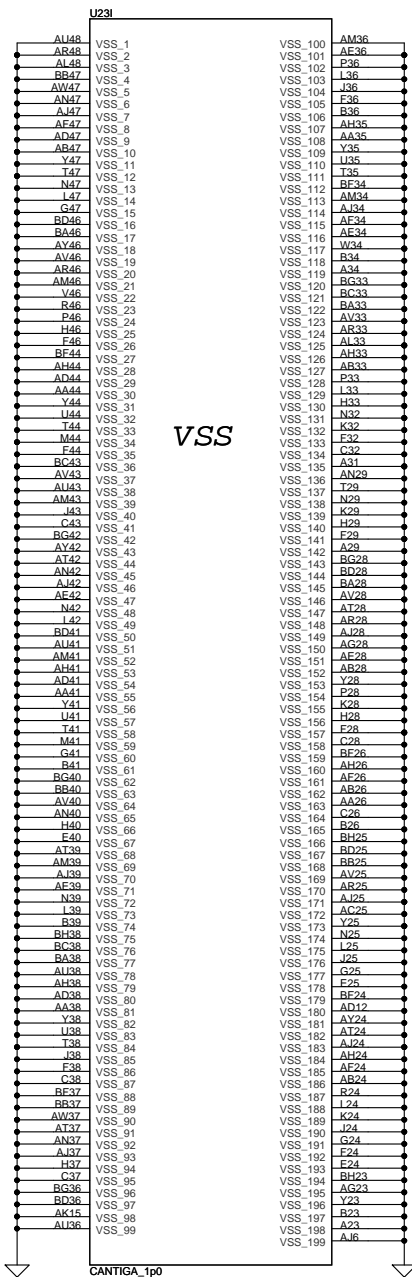




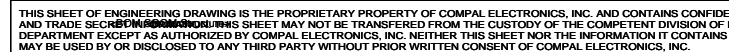




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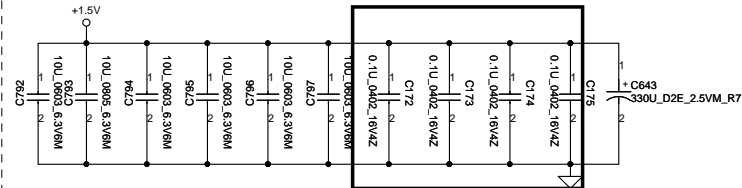
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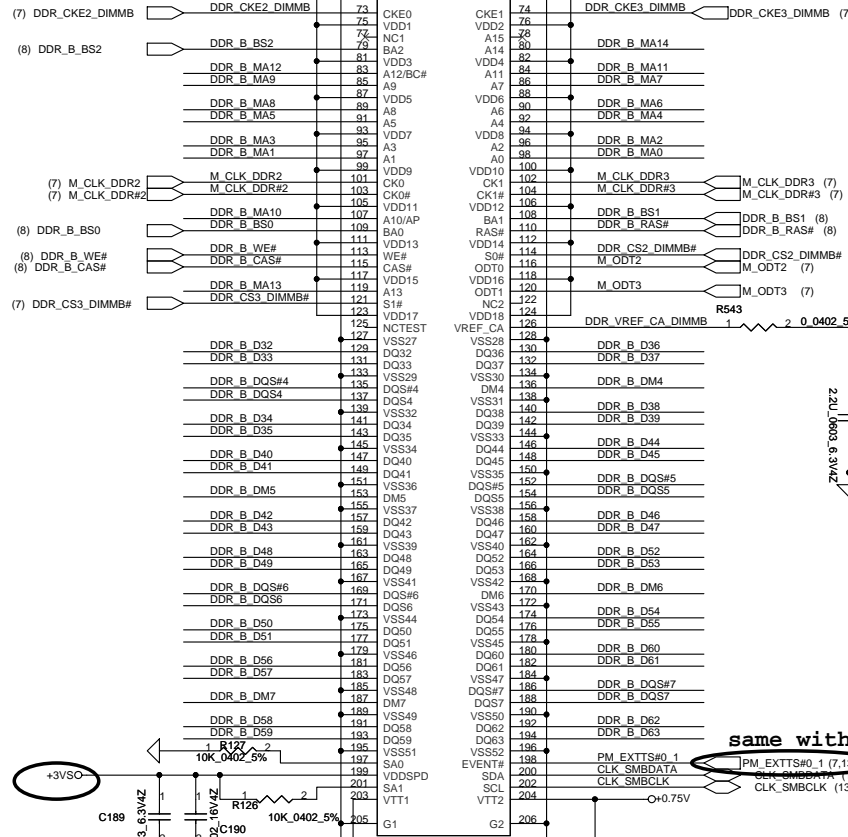
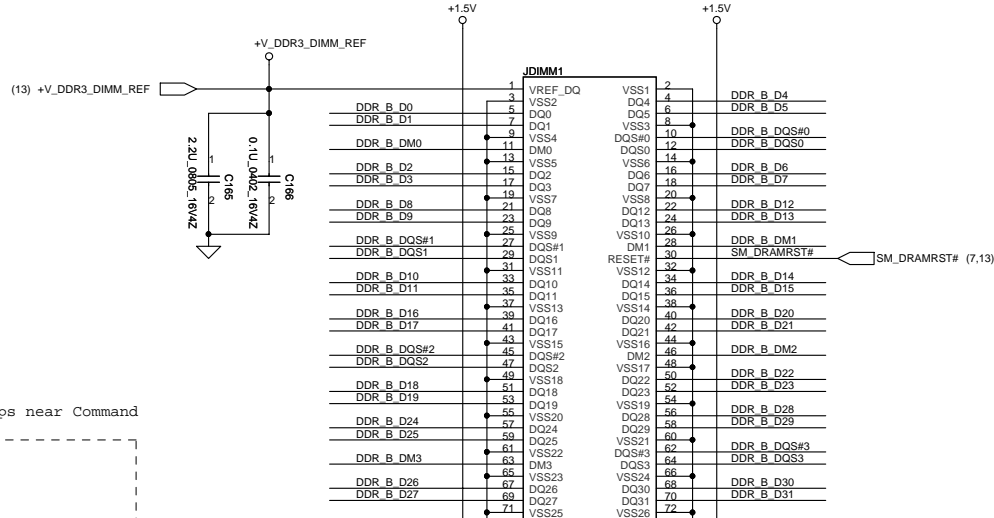
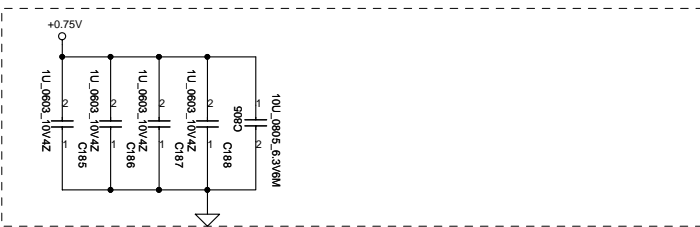
- (8) DDR\_B\_DQS#[0..7]
- (8) DDR\_B\_DQ[0..63]
- (8) DDR\_B\_DM[0..7]
- (8) DDR\_B\_DQS[0..7]
- (8) DDR\_B\_MA[0..14]

Layout Note:  
Place near JP5

Layout Note: Place these 4 Caps near Command  
and Control signals of DIMMA



Layout Note:  
Place near JP5.203 & JP5.204

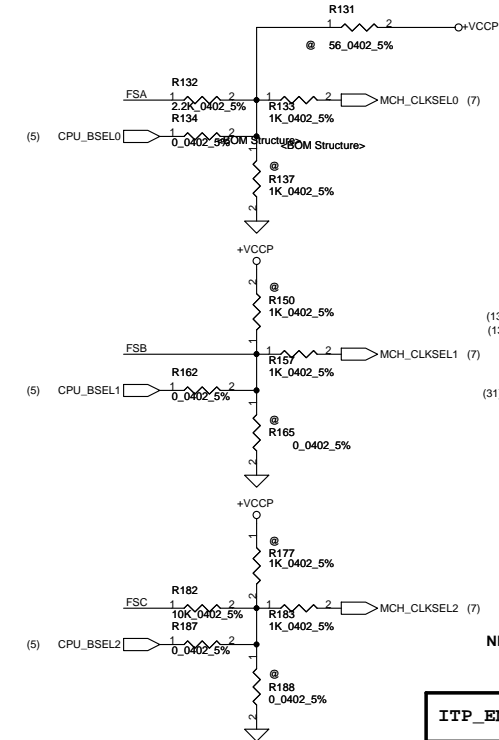
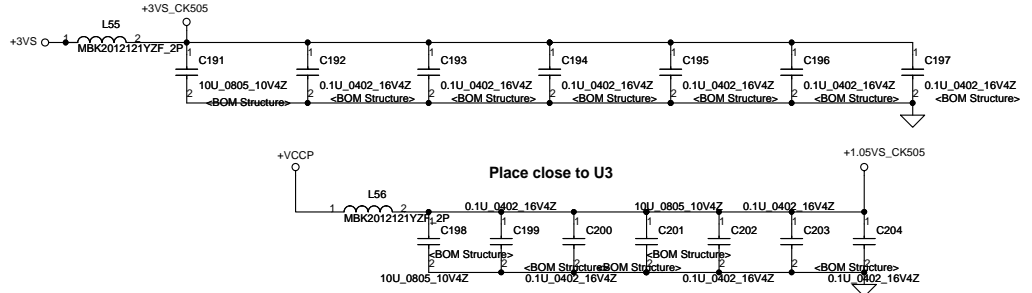
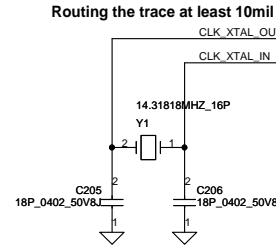


same with intel DDR3 CRB connection

DDR3 SO-DIMM B  
REVERSE

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FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



NB  
CPU

- (7) CLKREQ#\_7
- (7) CLK\_MCH\_BCLK#
- (7) CLK\_MCH\_BCLK#
- (4) CLK\_CPU\_BCLK#
- (4) CLK\_CPU\_BCLK#

(20) CK\_PWRGD

(20) CLK\_14M\_ICH

(13,14) CLK\_SMBDATA

(13,14) CLK\_SMBCLK

0905 Connect

PCI\_CLK

(31) CLK\_PCI\_EC

(18) PCI\_CLK

(28) CLK\_SD\_48M

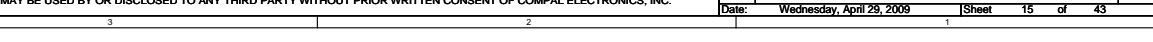
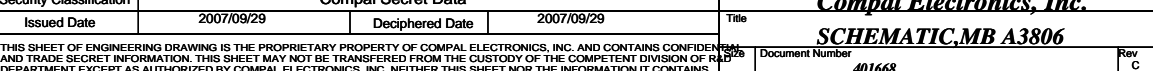
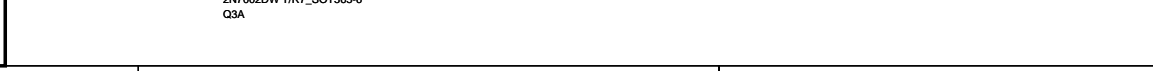
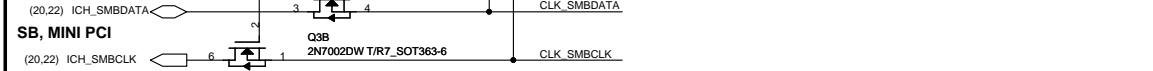
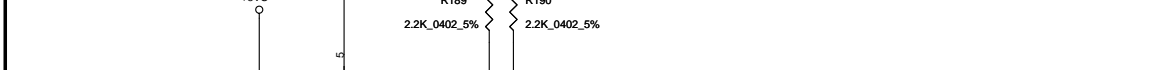
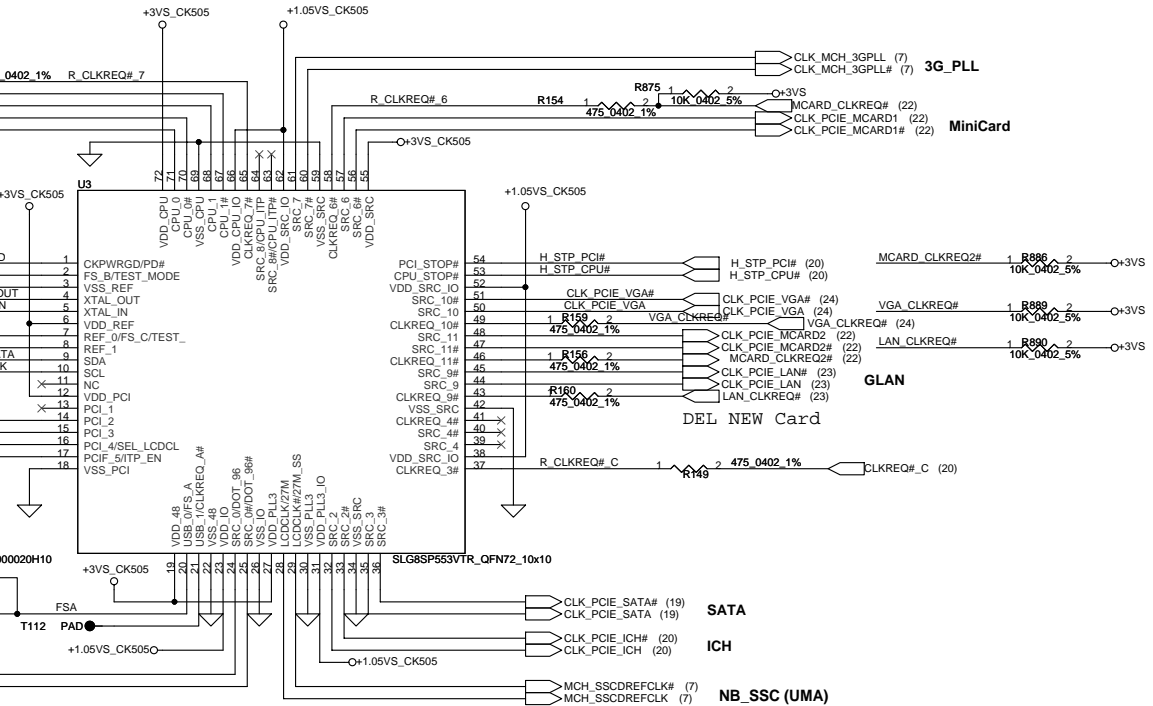
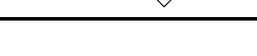
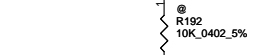
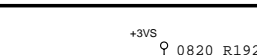
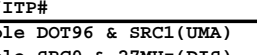
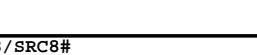
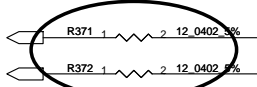
(20) CLK\_48M\_ICH

(7) CLK\_MCH\_DREFCLK

(7) CLK\_MCH\_DREFCLK#

NB (UMA)

2008/10/07  
Add 48M for Card reader



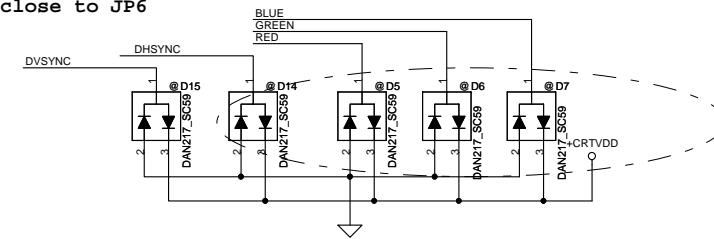
for ICS Overclocking setting  
0=Overclocking of CPU and SRC allowed  
1=Overclocking of CPU and SRC NOT allowed

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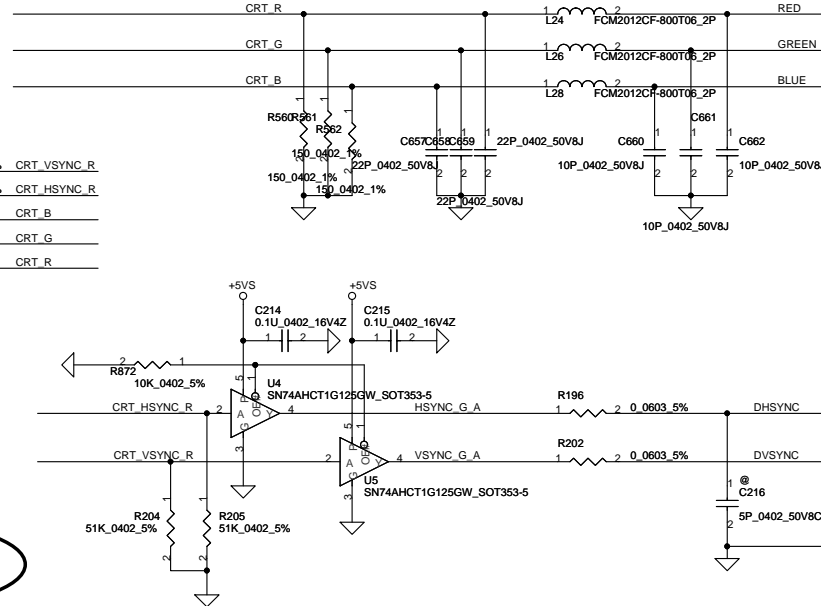
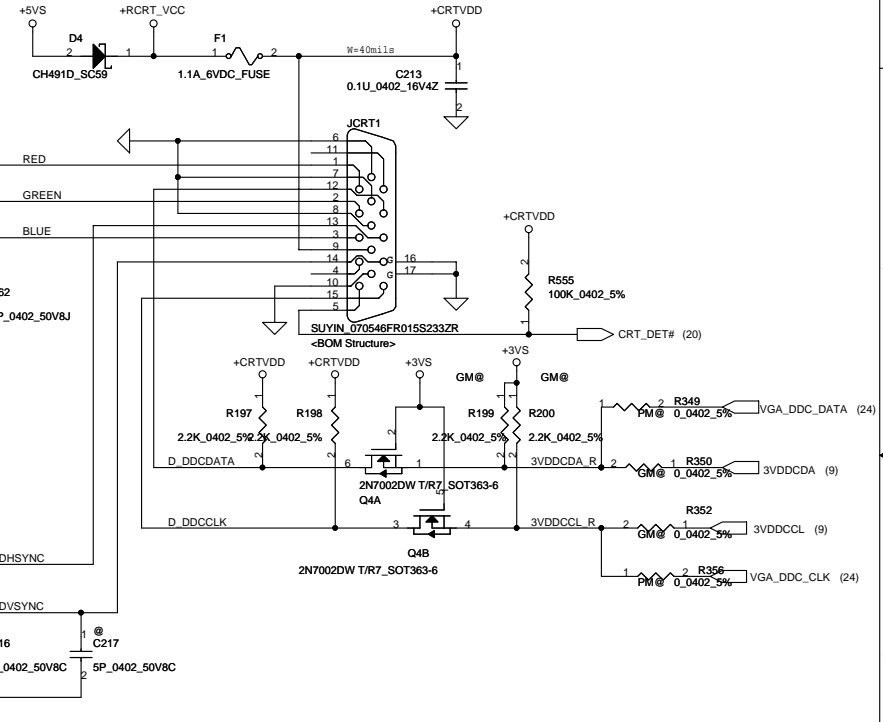
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Place close to JP6

NOTE: L :  $A \rightarrow B1$   
H:  $A \rightarrow B2$



## CRT Connector



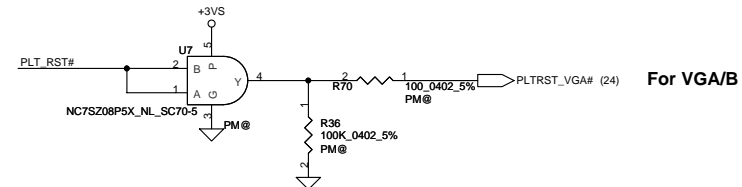
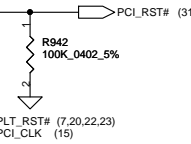
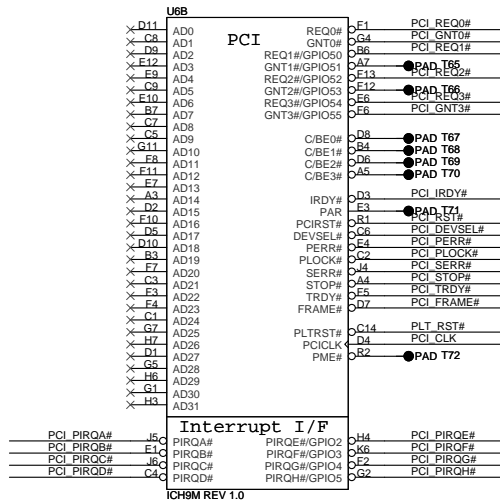
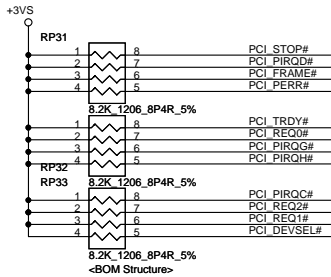
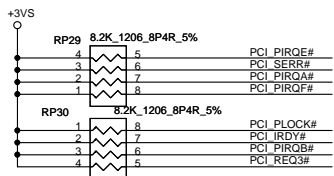
(9)	CRT_VSYNC		CRT_VSYNC	R61	1	<del>CME</del>	2	30.1_0402 1%	CRT_VSYNC_R
(9)	CRT_HSYNC		CRT_HSYNC	R69	1	<del>CME</del>	2	30.1_0402 1%	CRT_HSYNC_R
(9)	M_BLUE		M_BLUE	R328	1	<del>CME</del>	2	0_0402 5%	CRT_B
(9)	M_GREEN		M_GREEN	R330	1	<del>CME</del>	2	0_0402 5%	CRT_G
(9)	M_RED		M_RED	R332	1	<del>CME</del>	2	0_0402 5%	CRT_R

(24)	VGA_CRT_VSYNC	R65	1	PM@ 0.0402 5%	CRT_VSYNC_R
(24)	VGA_CRT_HSYNC	R67	1	PM@ 0.0402 5%	CRT_HSYNC_R
(24)	VGA_CRT_B	R333	1	PM@ 0.0402 5%	CRT_B
(24)	VGA_CRT_G	R334	1	PM@ 0.0402 5%	CRT_G
(24)	VGA_CRT_R	R335	1	PM@ 0.0402 5%	CRT_R

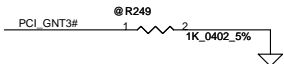
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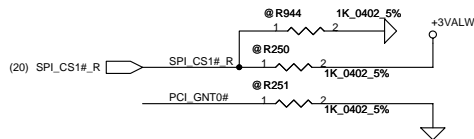


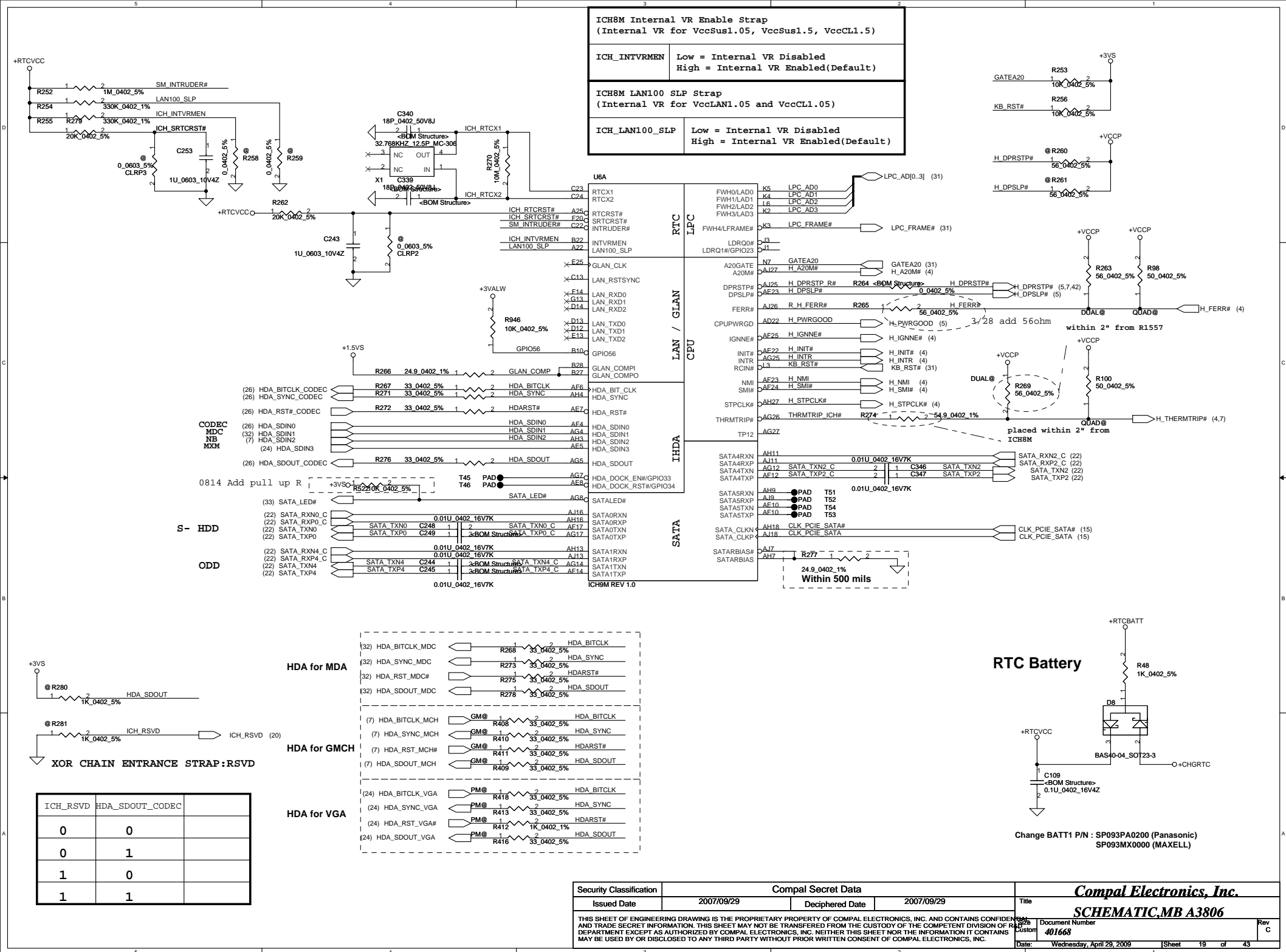


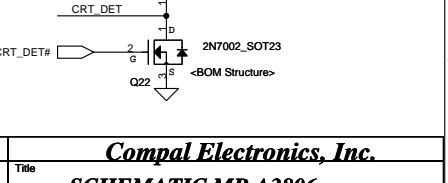
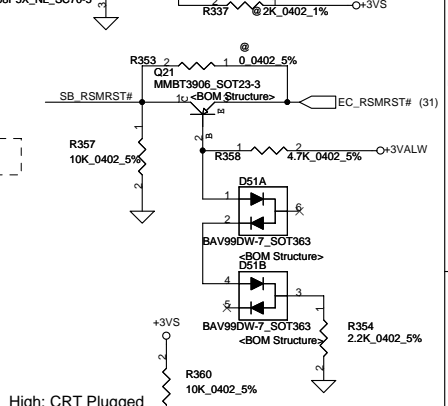
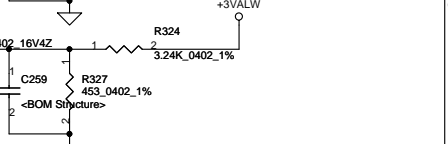
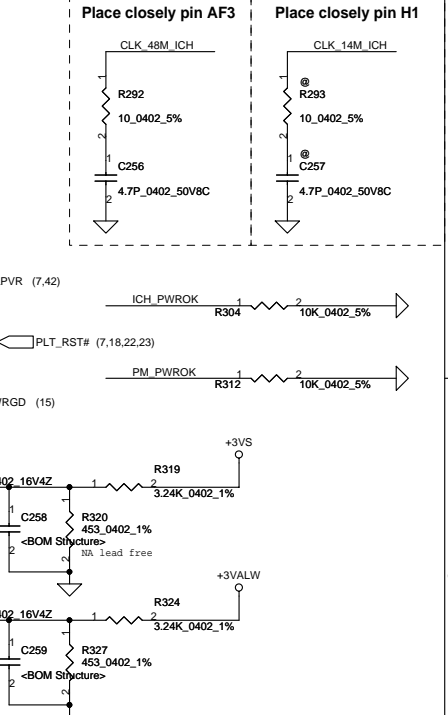
A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enble High= Default *



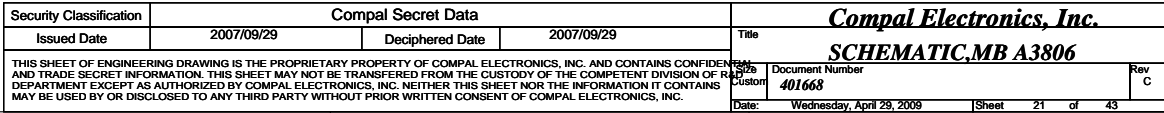
Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *



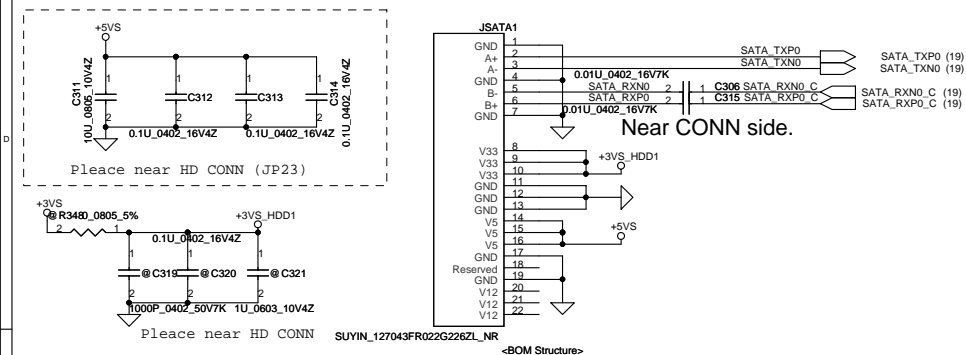




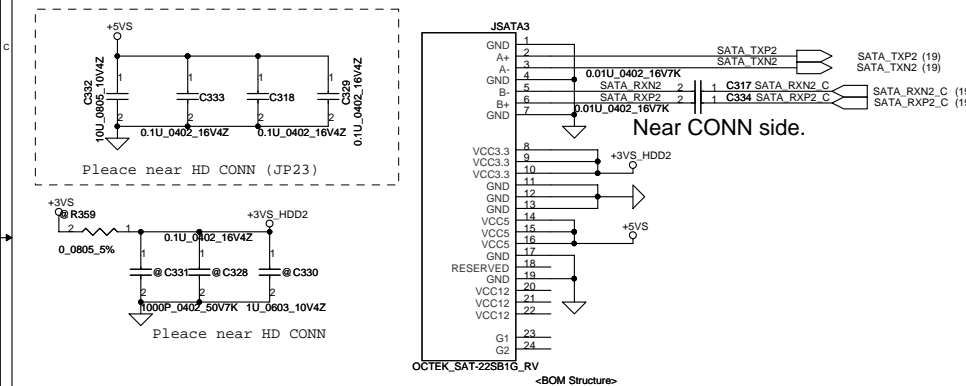
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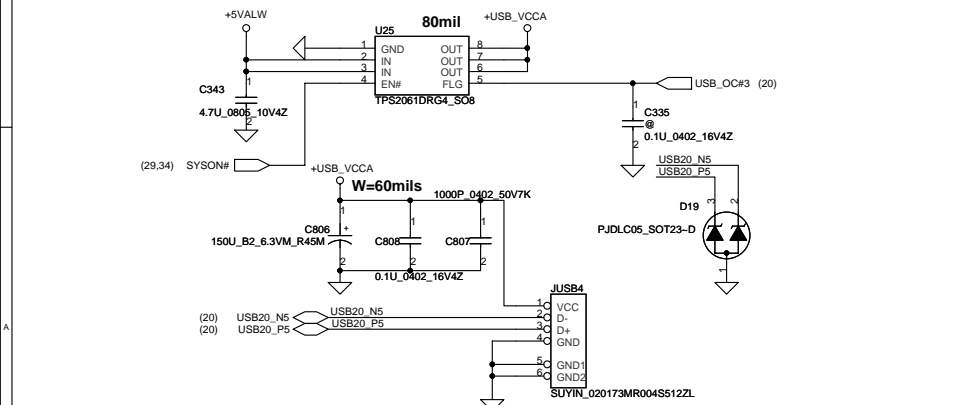
## HDD Connector



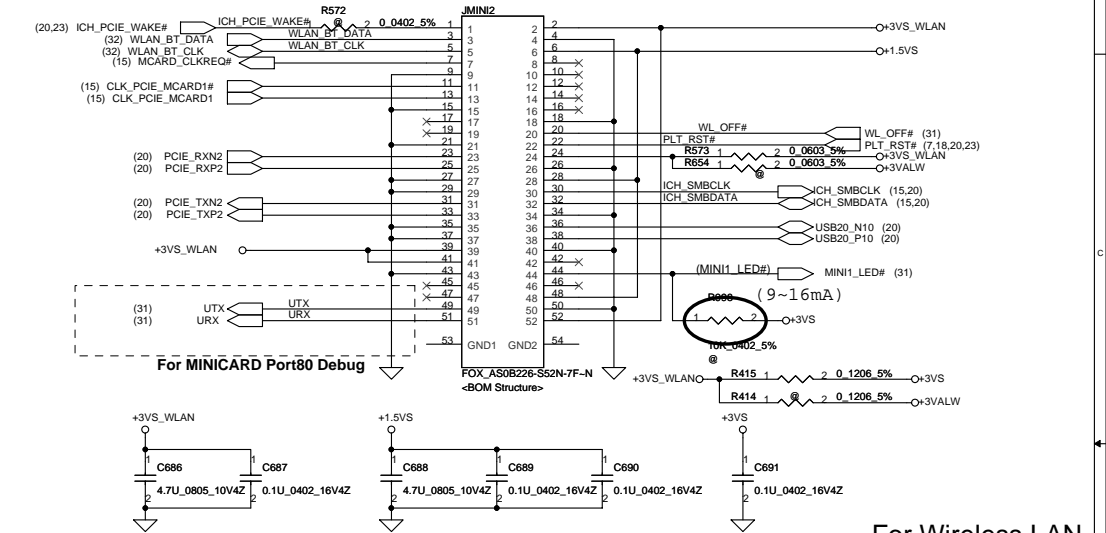
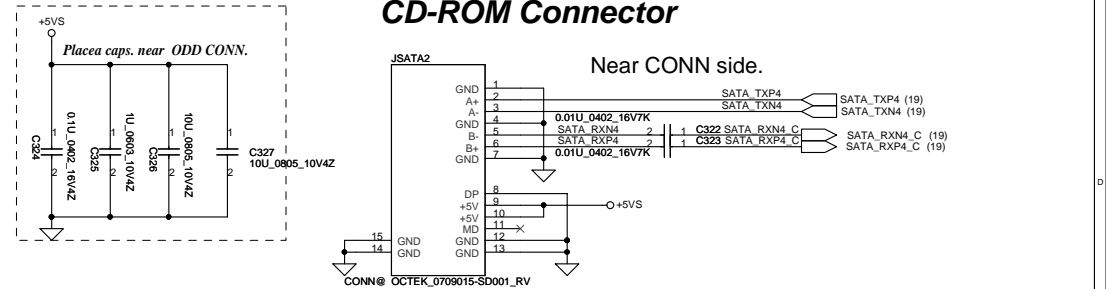
## HDD Connector



## eSATA w/ USB port

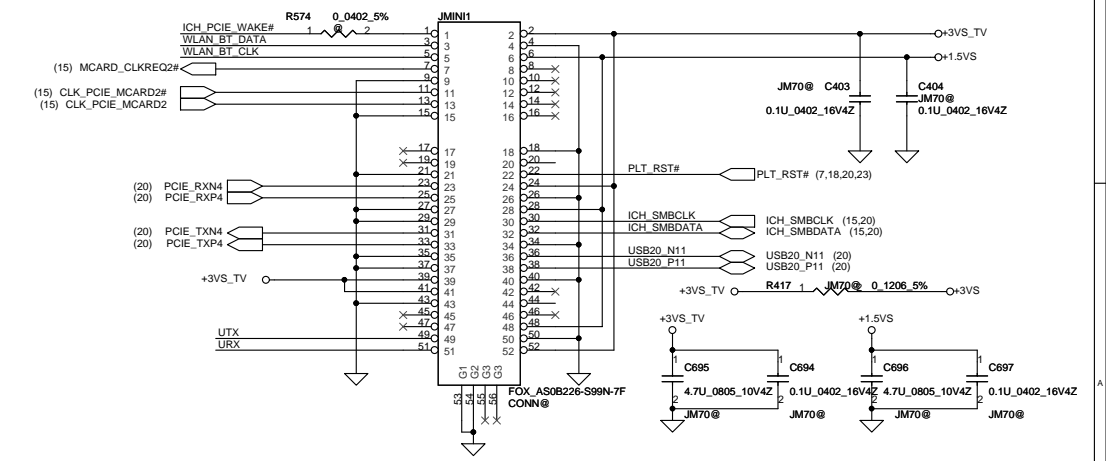


## CD-ROM Connector

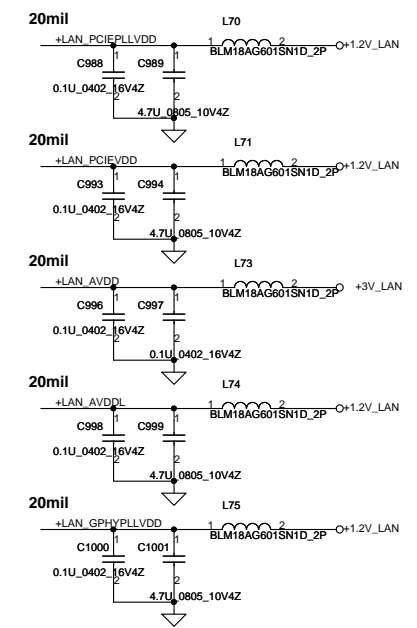
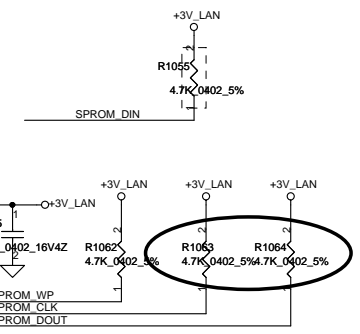
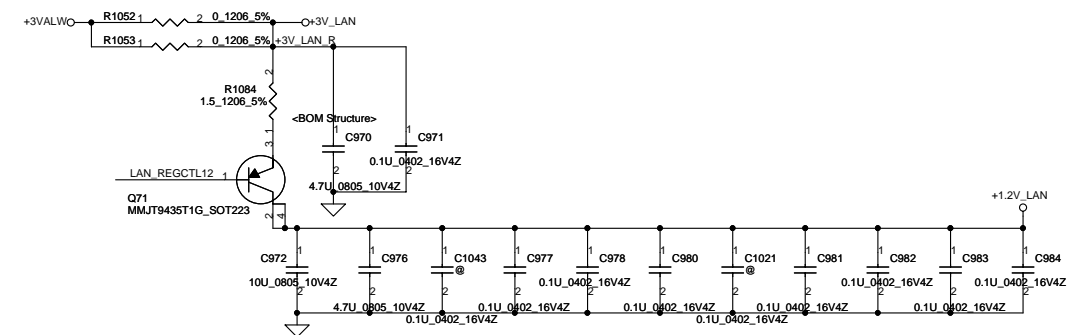
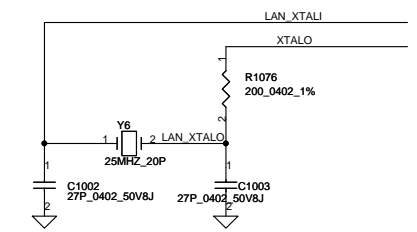
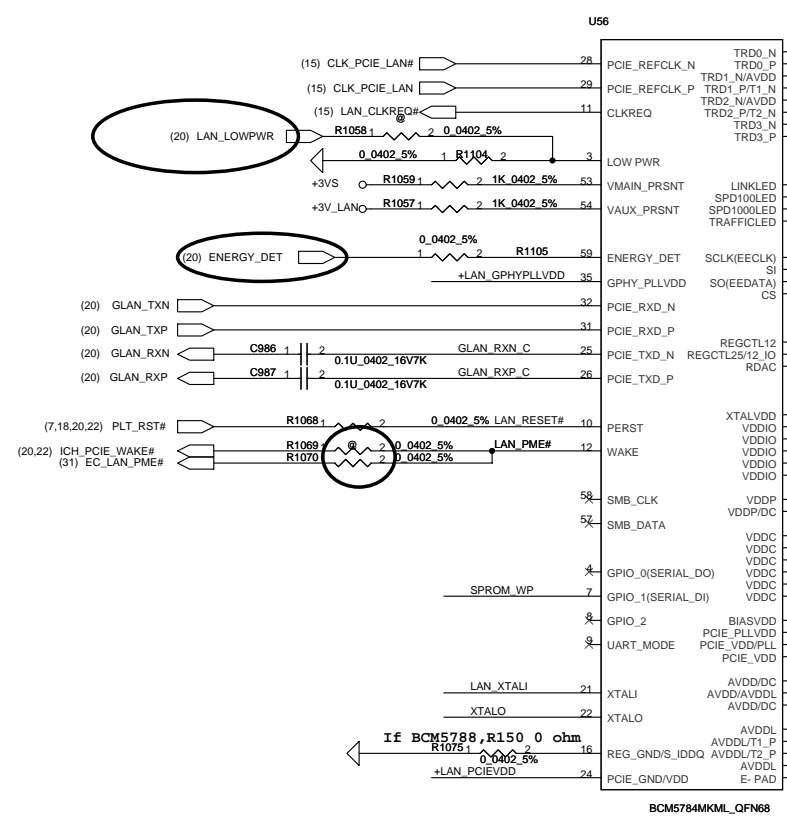
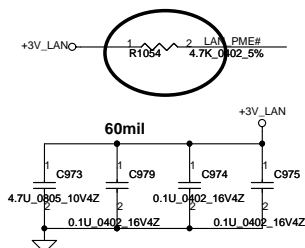


For Wireless LAN

For TV Tuner

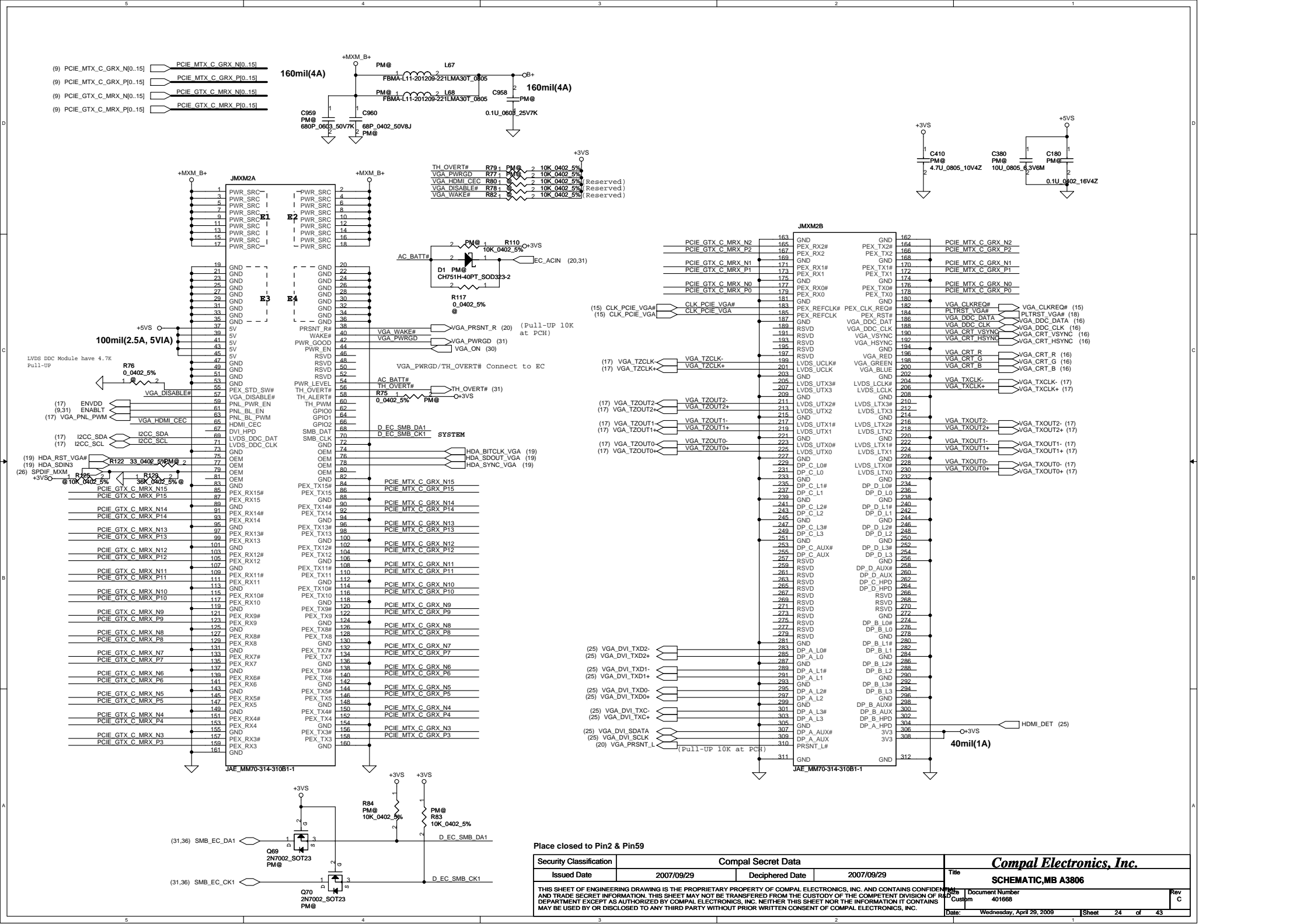


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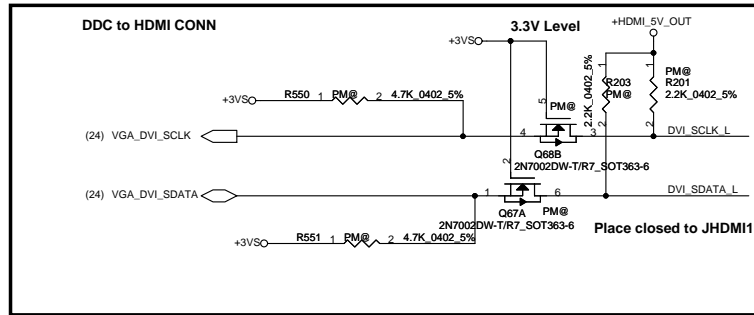
Place closed to Pin2 & Pin59

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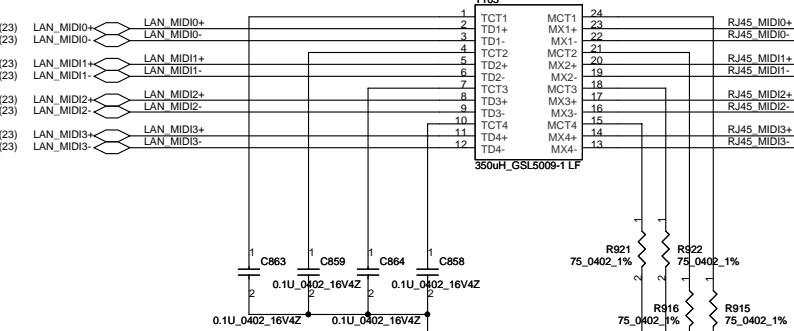
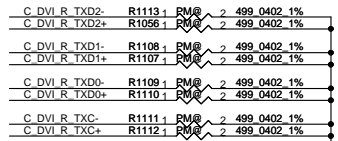
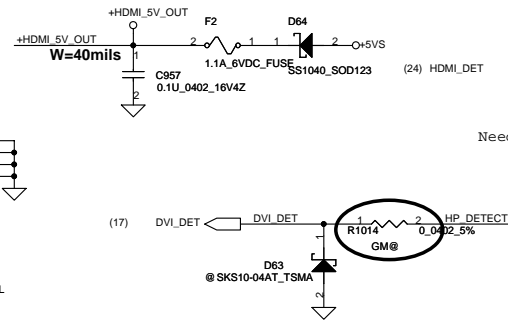
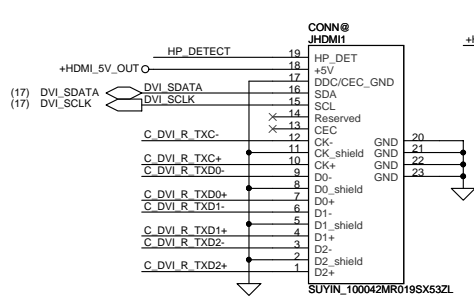




Need Check

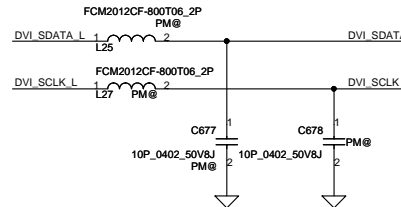
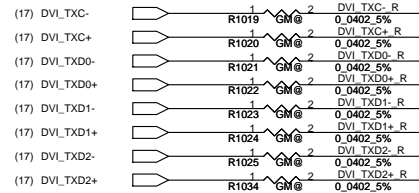


## HDMI Connector



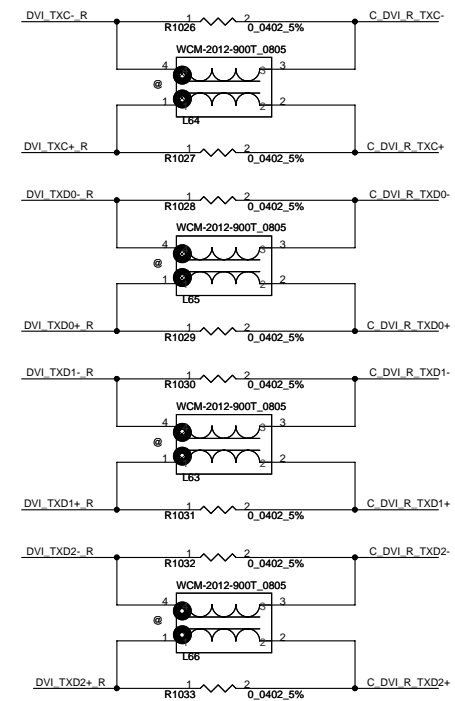
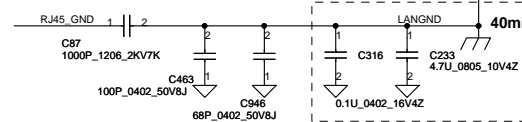
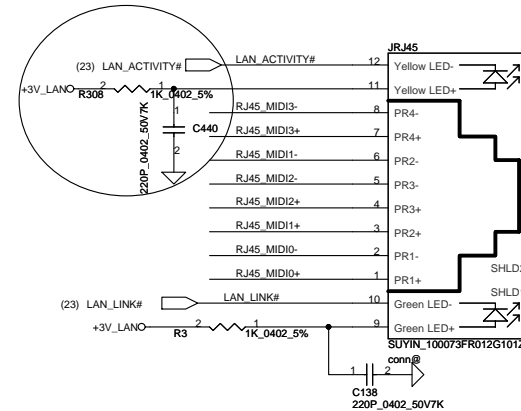
Place close to TCT pin

40mil



Need Check

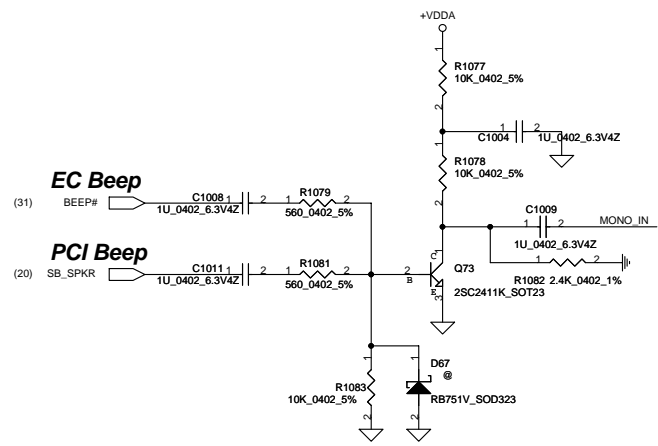
Need CHECK



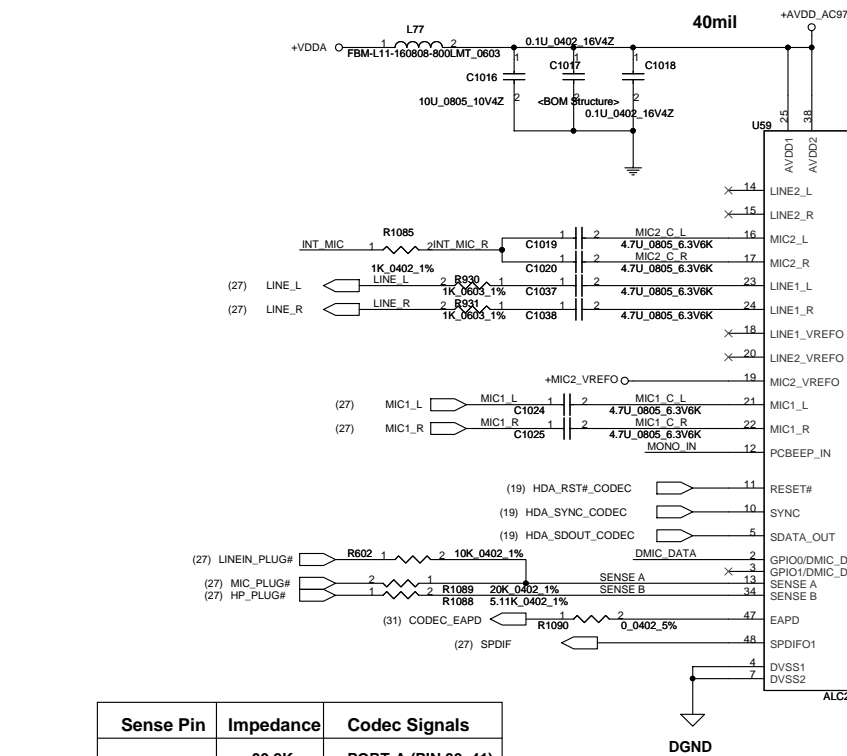
Guide Pin

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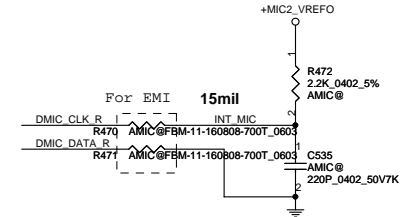
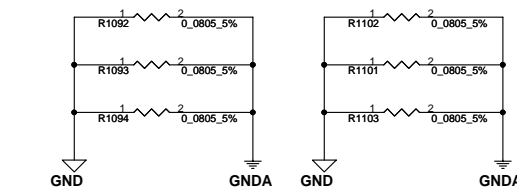
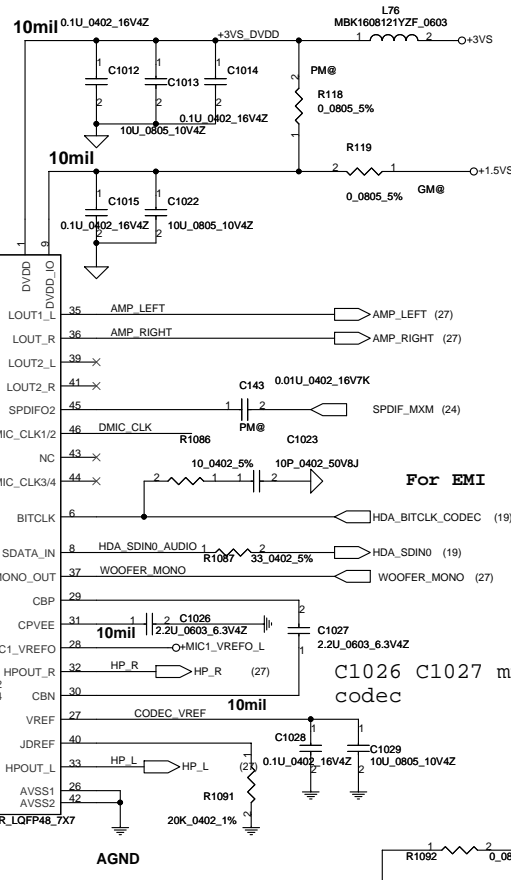
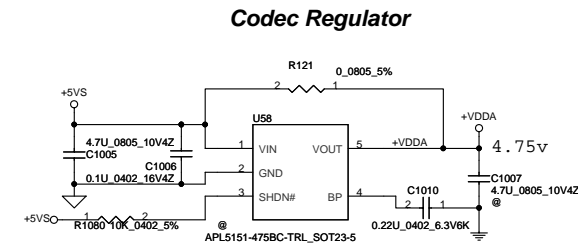
SCHEMATIC.MB A3806



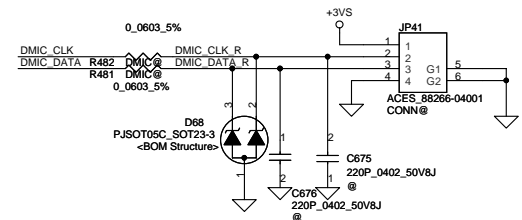
## HD Audio Codec



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



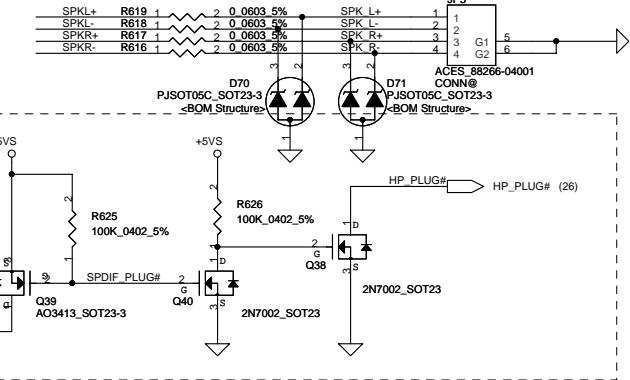
## DMIC Conn.



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# Int. Speaker Conn.

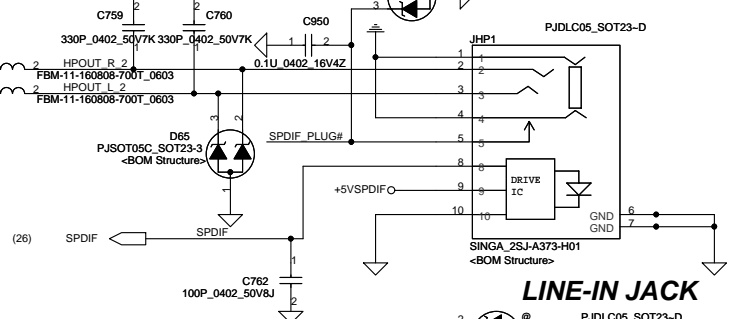
20mil



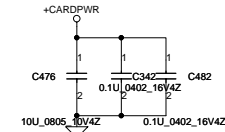
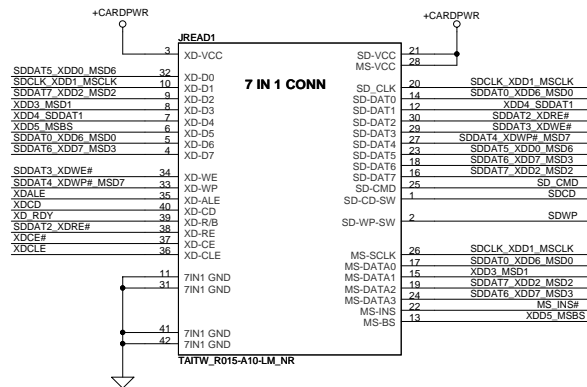
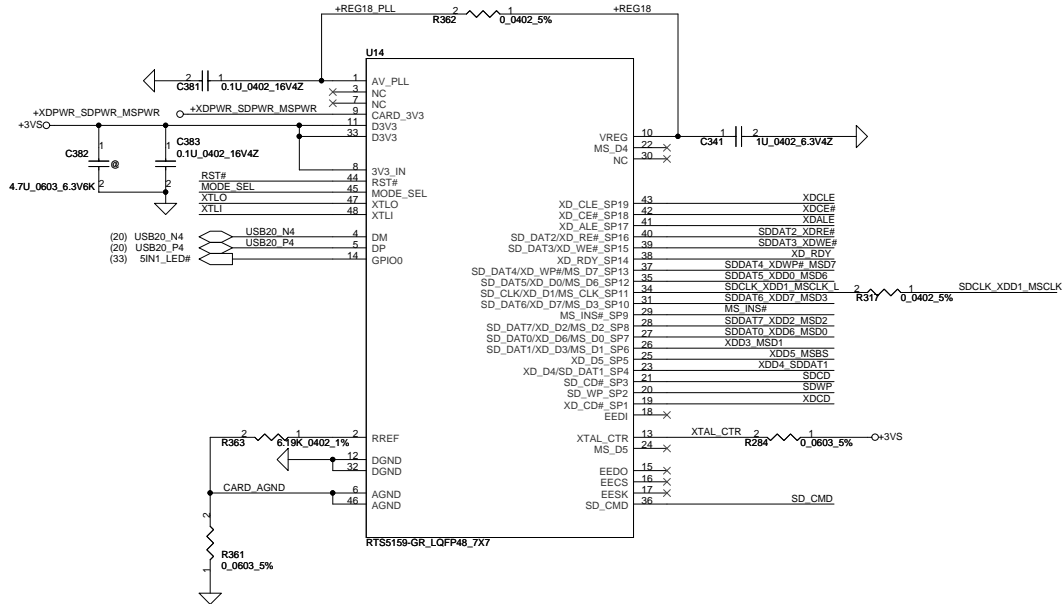
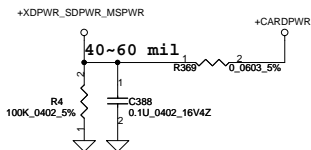
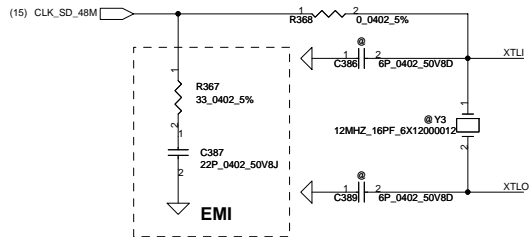
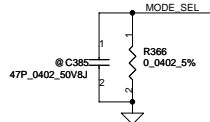
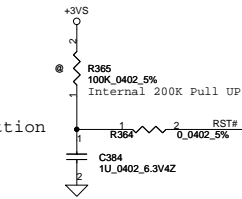
LINE Out/Headphone Out

2007/12/07 S/PDIF Out JACK

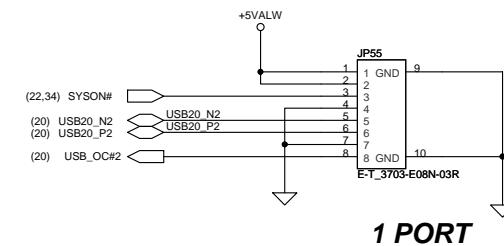
20mil



Vender suggestion

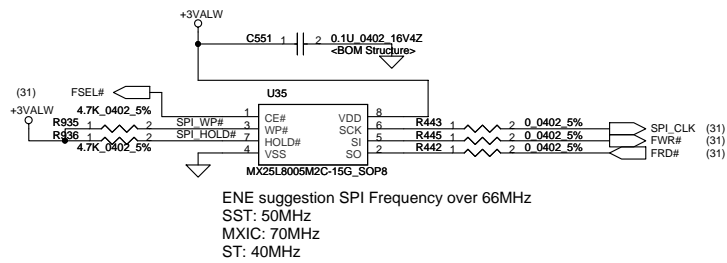


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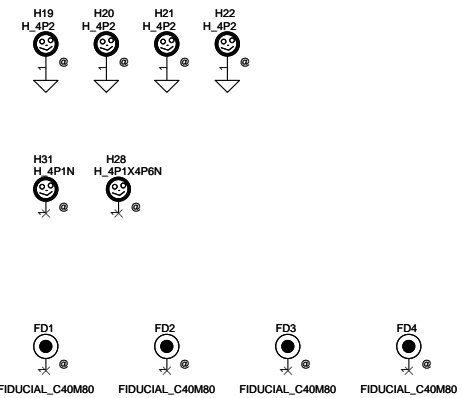
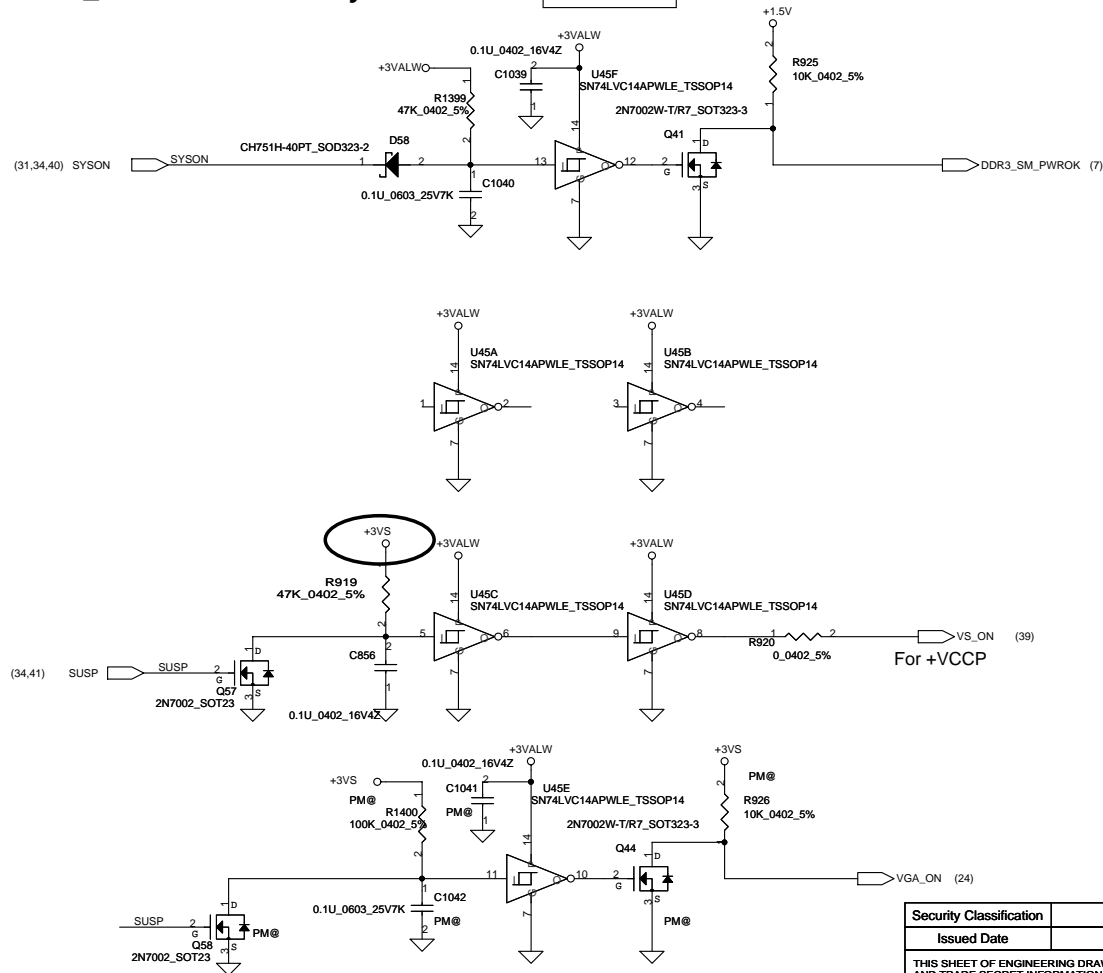
## BIOS



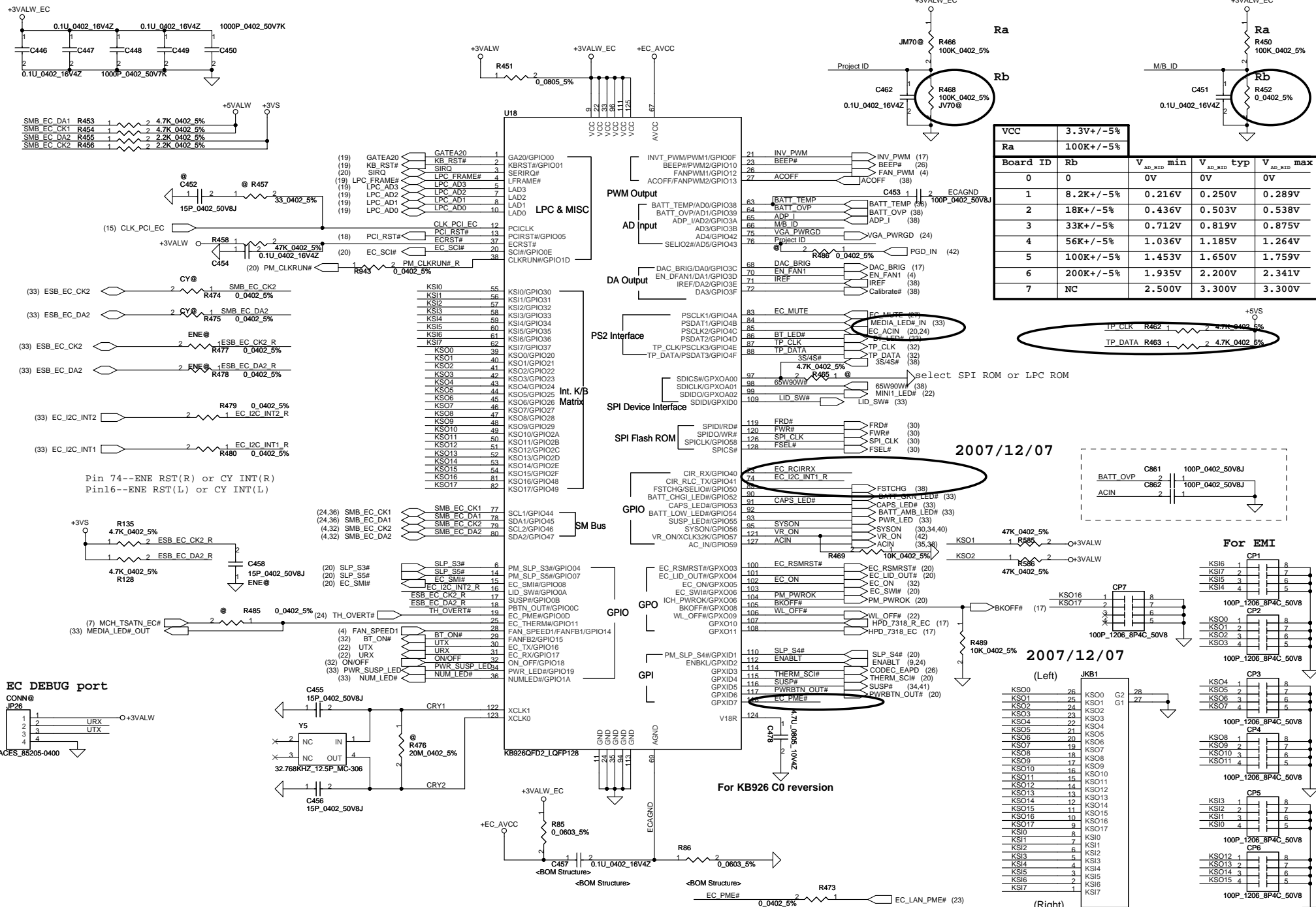
***VS\_ON will be driven by EC***

**reserve**

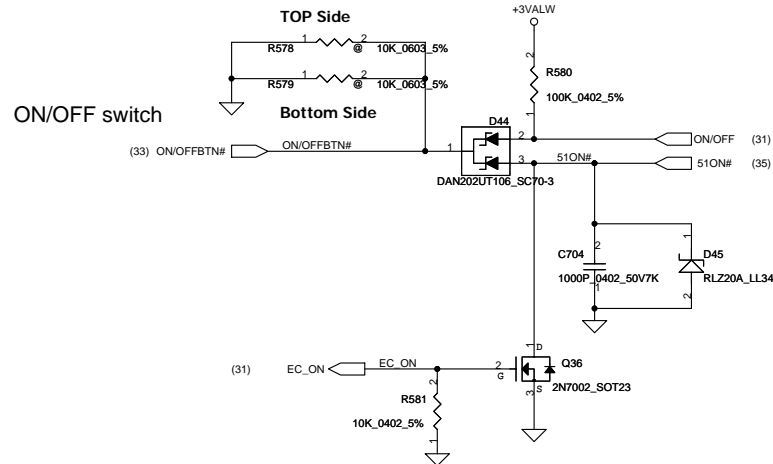
### ***Power ON Circuit***



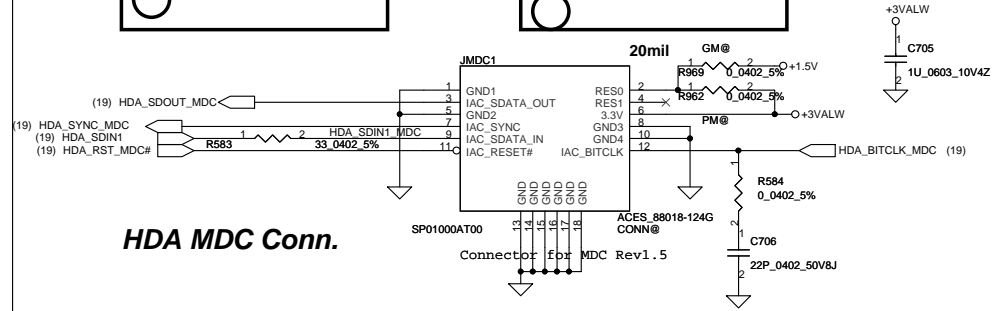
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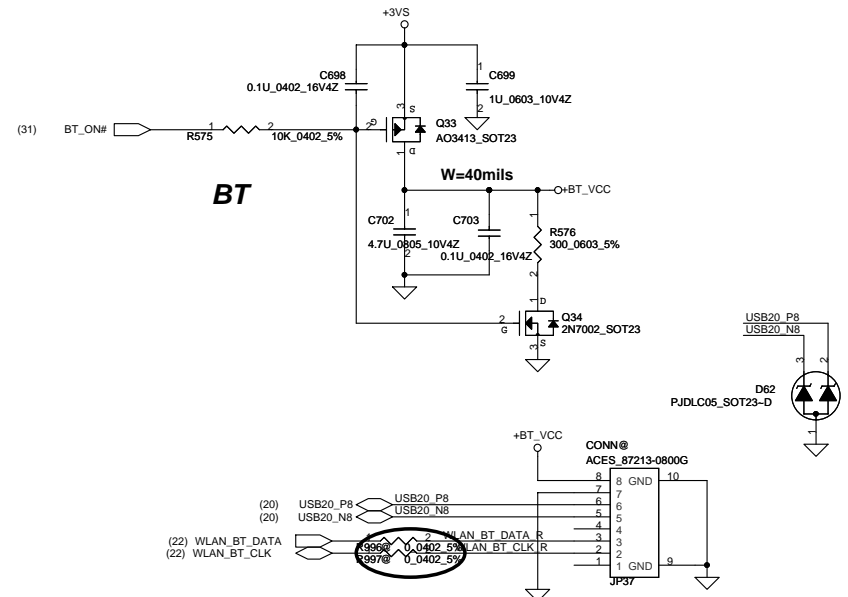
## Power Button



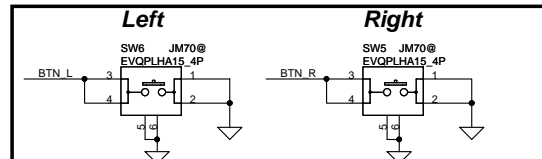
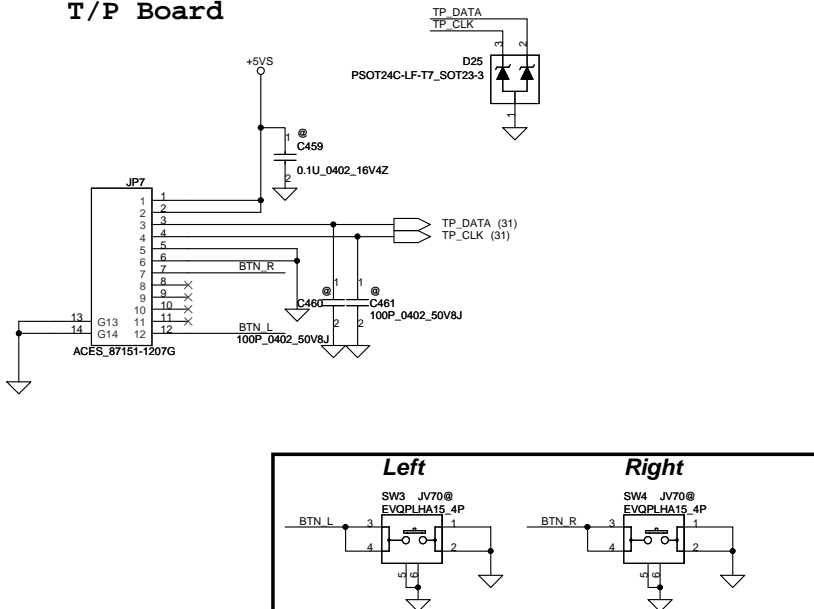
## HDA MDC Conn.



## BT



## T/P Board

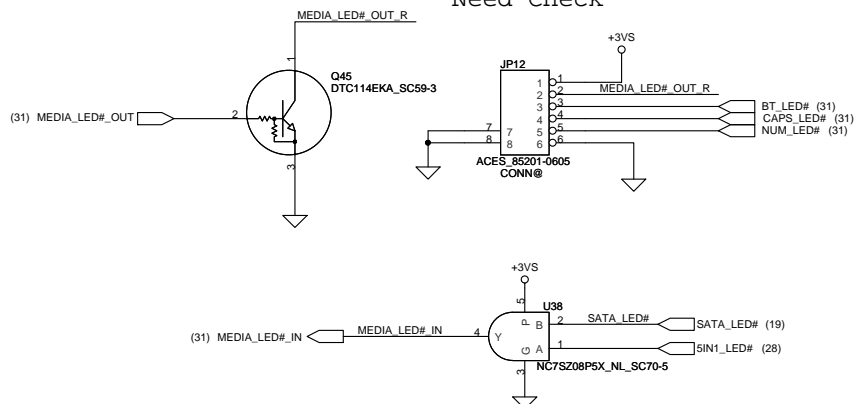


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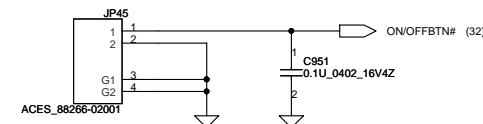
## LED/B

Need Check

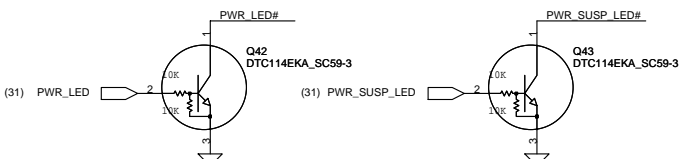


JM70	JV70
1.HDD	1.HDD
2.B/T	2.BT_LED
3.CAP LED	4.NUM LED
4.NUM_LED	3.CAP LED

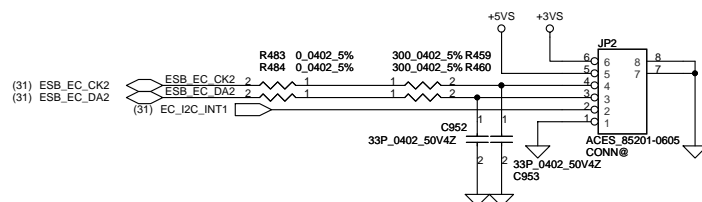
## POWER BOARD



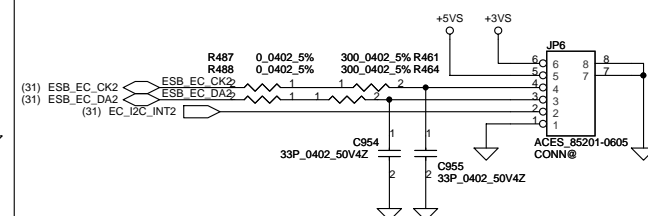
## Compal Footprint



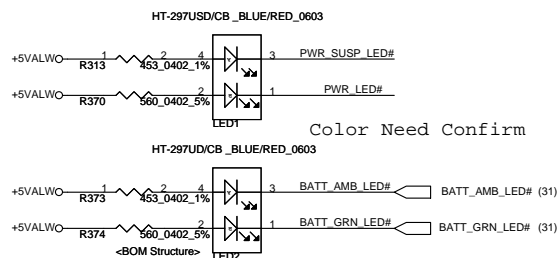
## CAP Sansor right



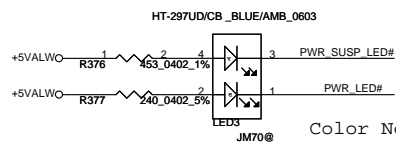
## CAP Sansor lift



## Color Need Confirm

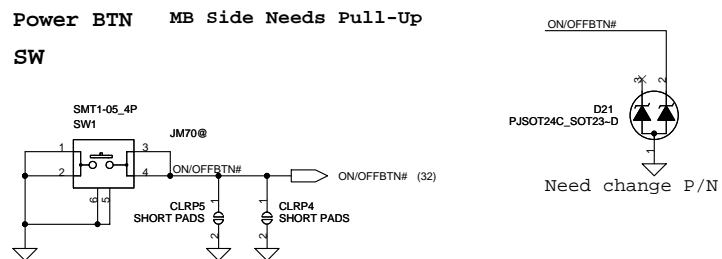
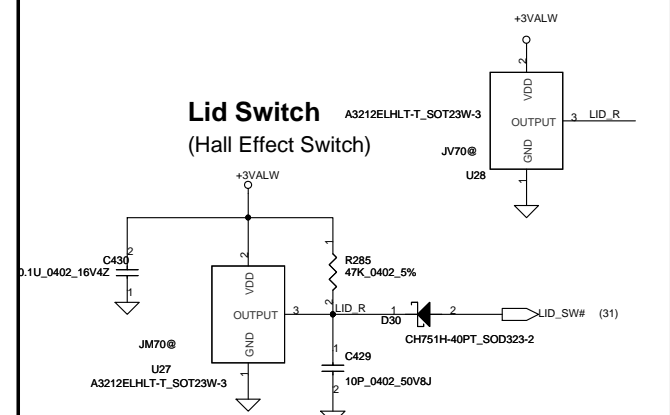


## Color Need Confirm

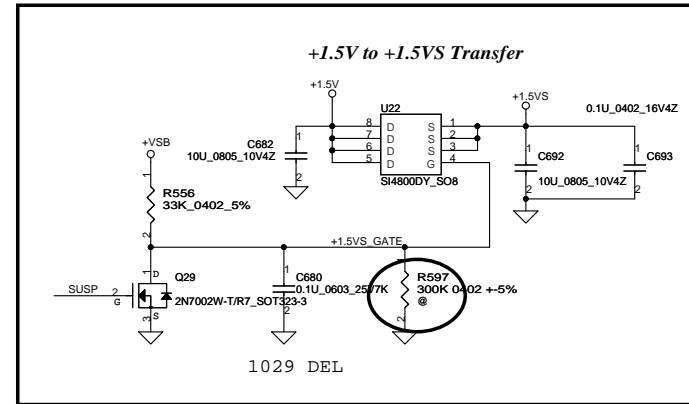
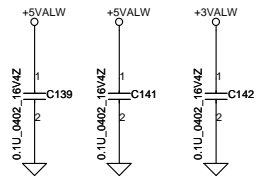
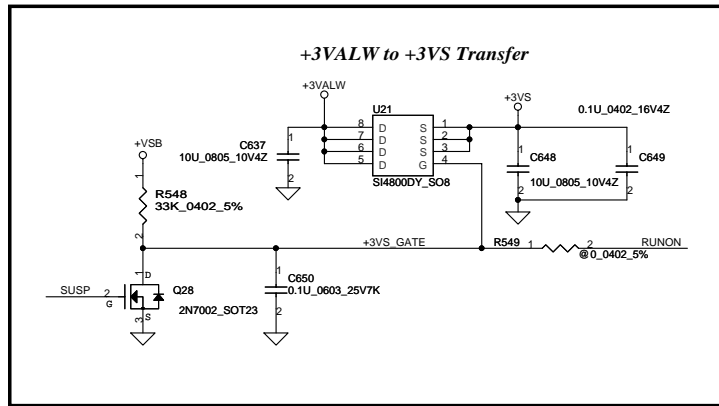
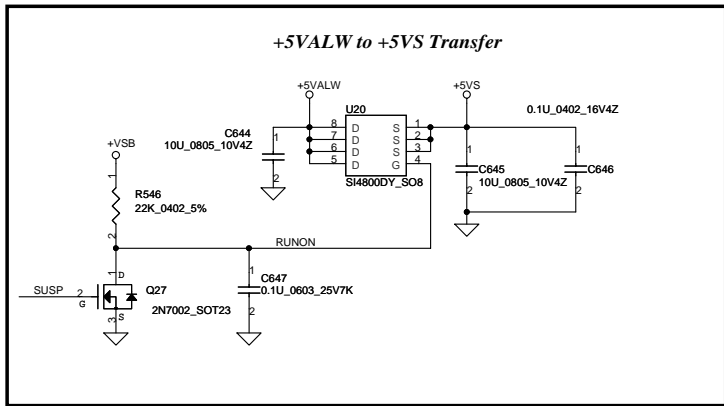


## Power BTN MB Side Needs Pull-Up

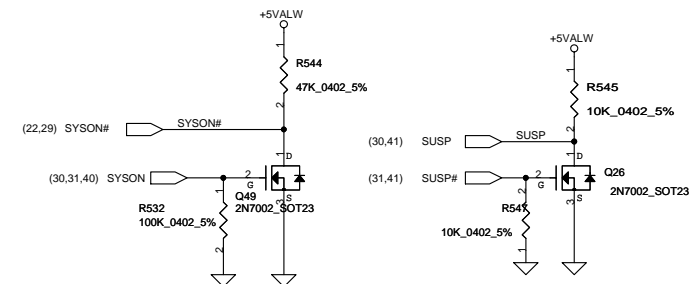
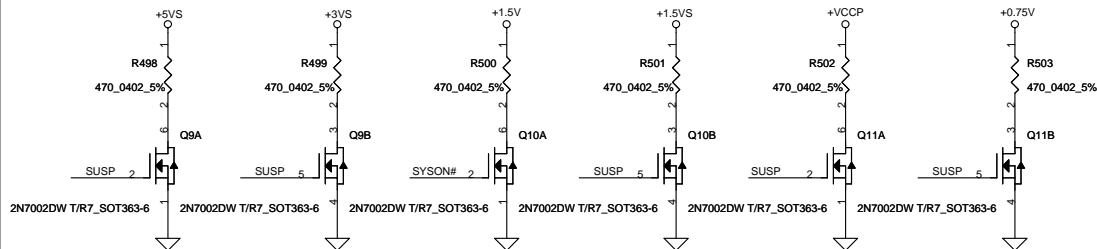
## SW

Lid Switch  
(Hall Effect Switch)

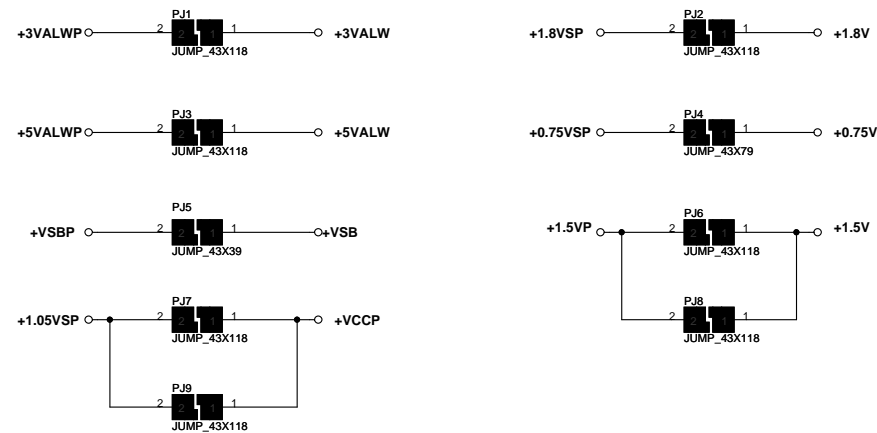
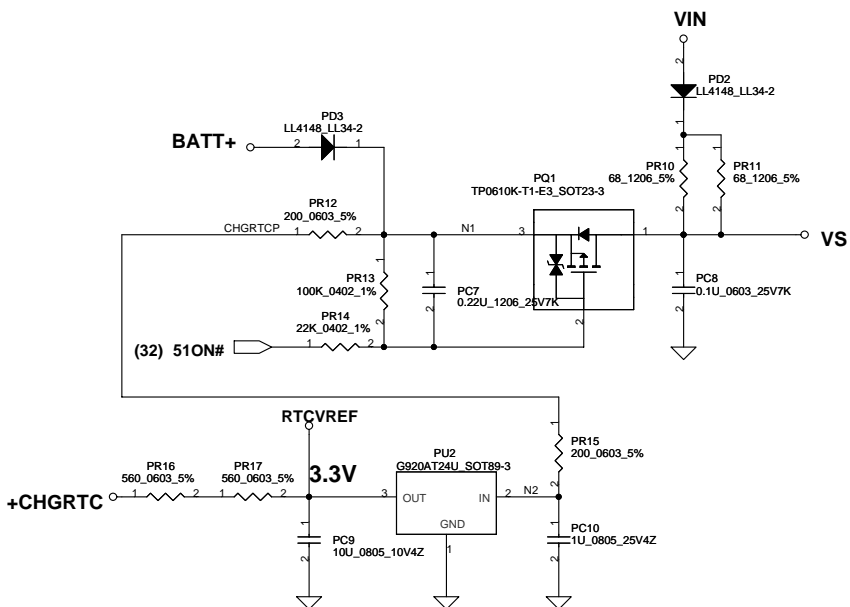
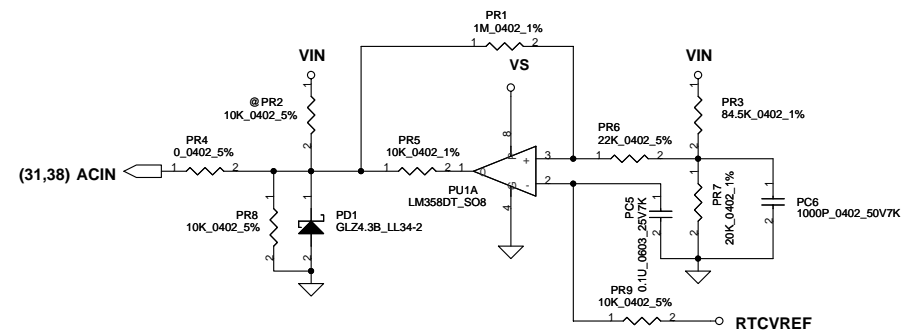
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### Discharge circuit

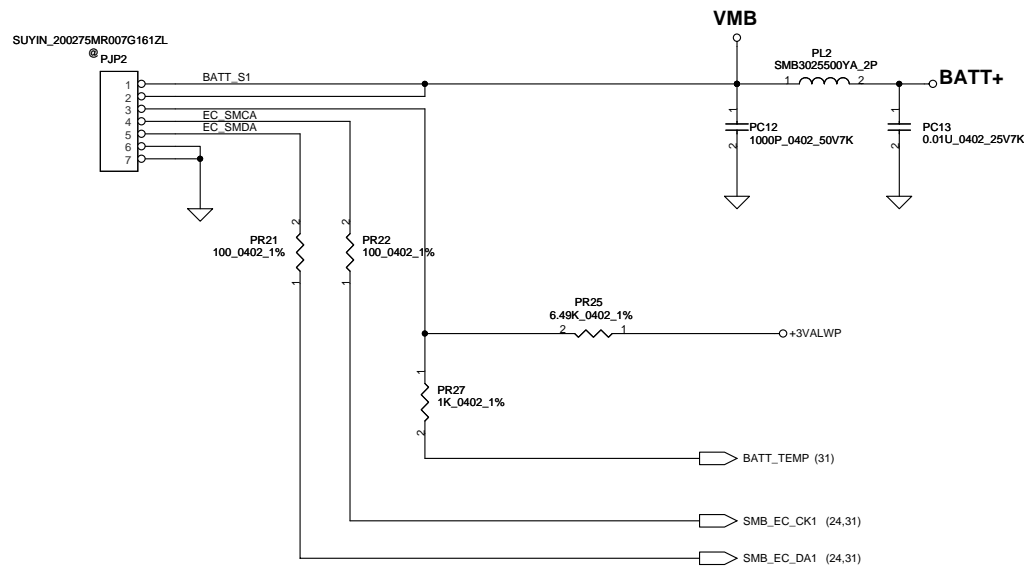


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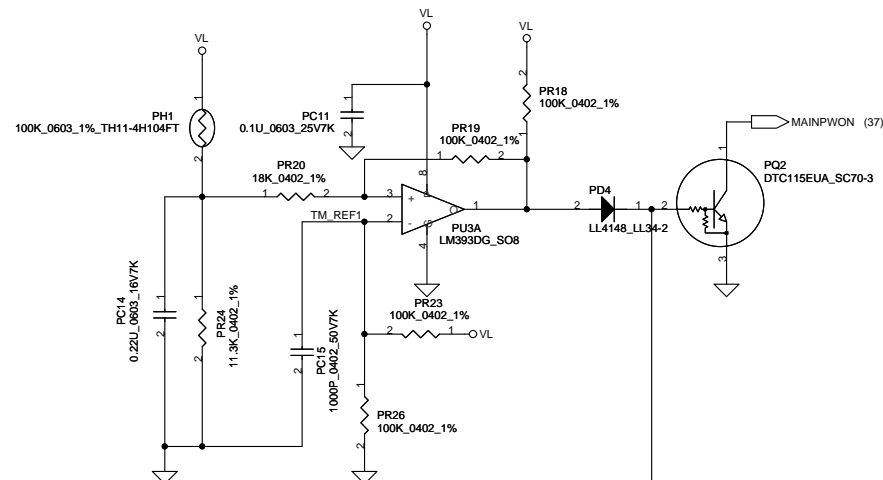


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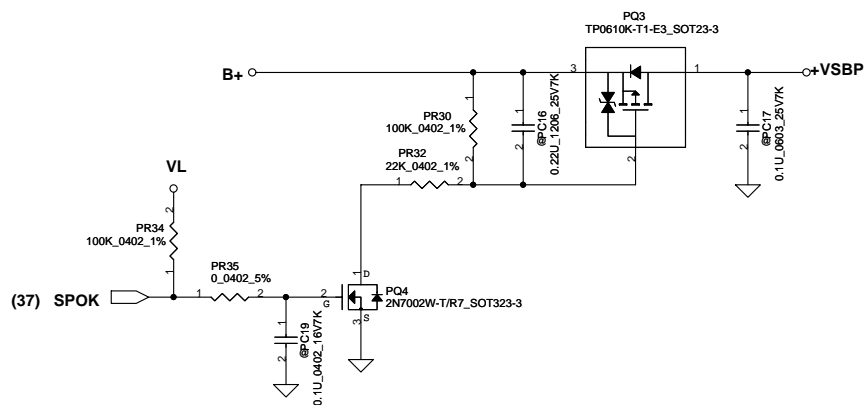
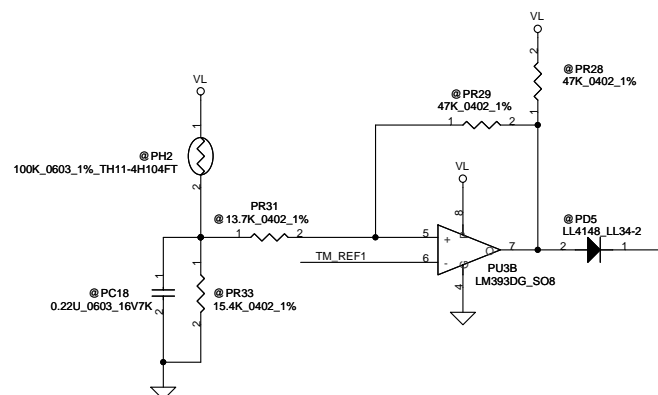
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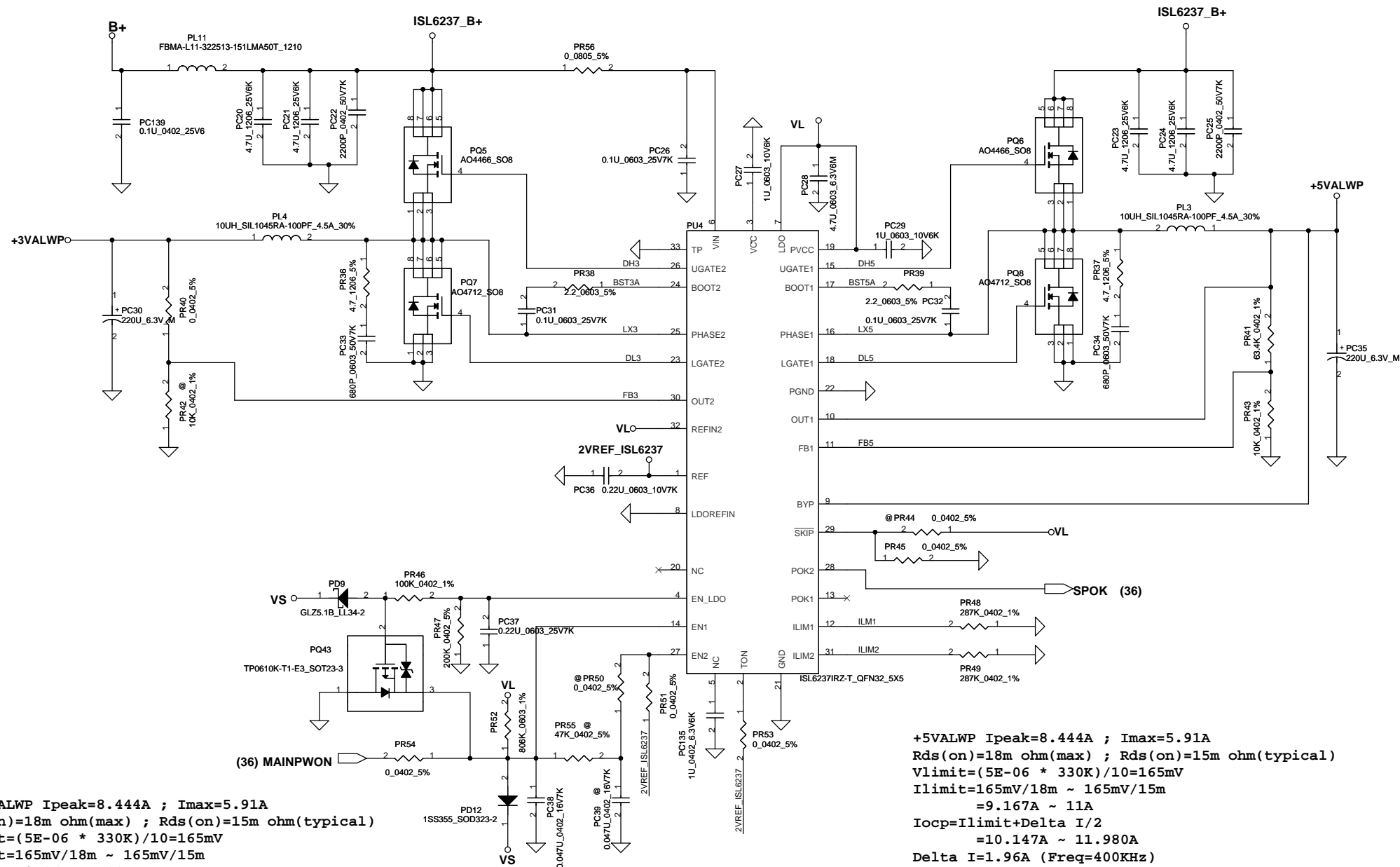
**PH1 under CPU botten side :**  
CPU thermal protection at 92 degree C  
Recovery at 70 degree C



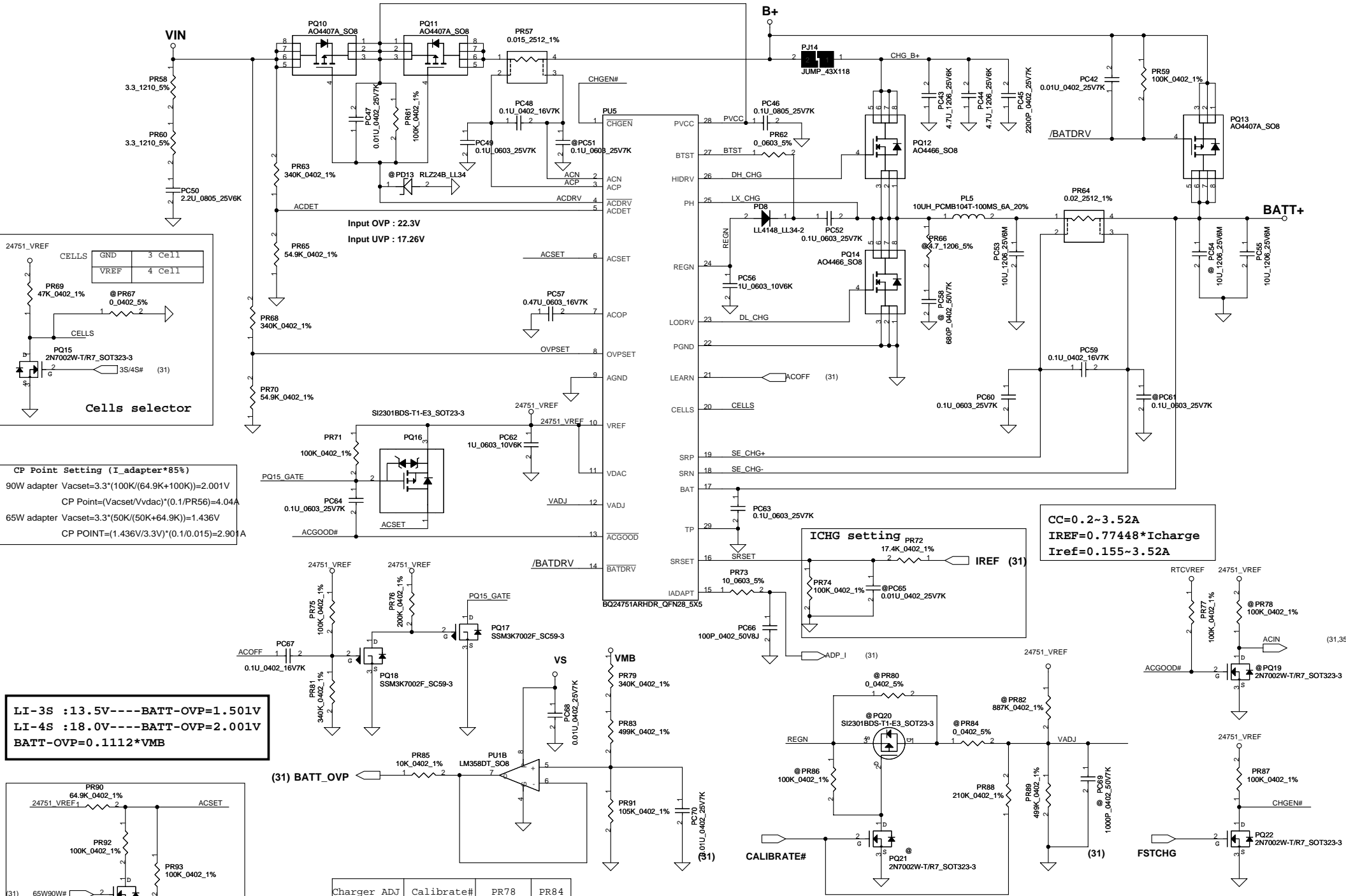
**PH2 near main Battery CONN :**  
BAT. thermal protection at 92 degree C  
Recovery at 56 degree C



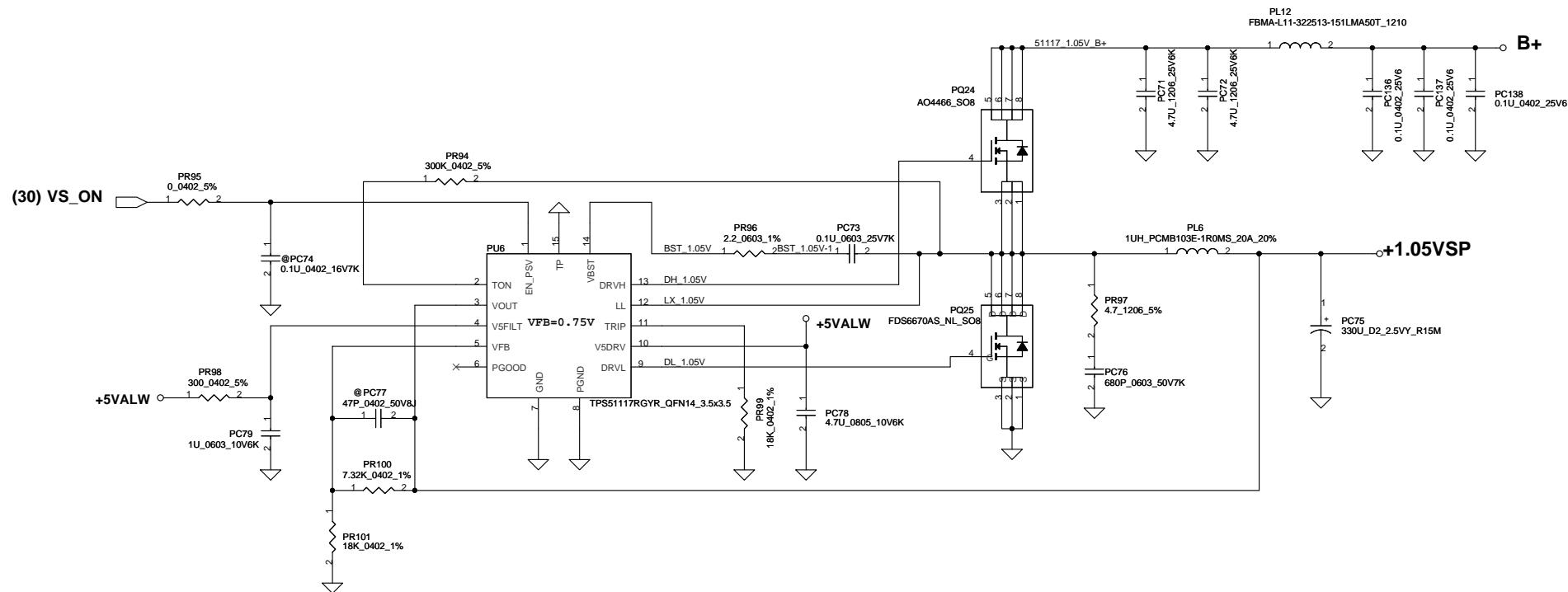
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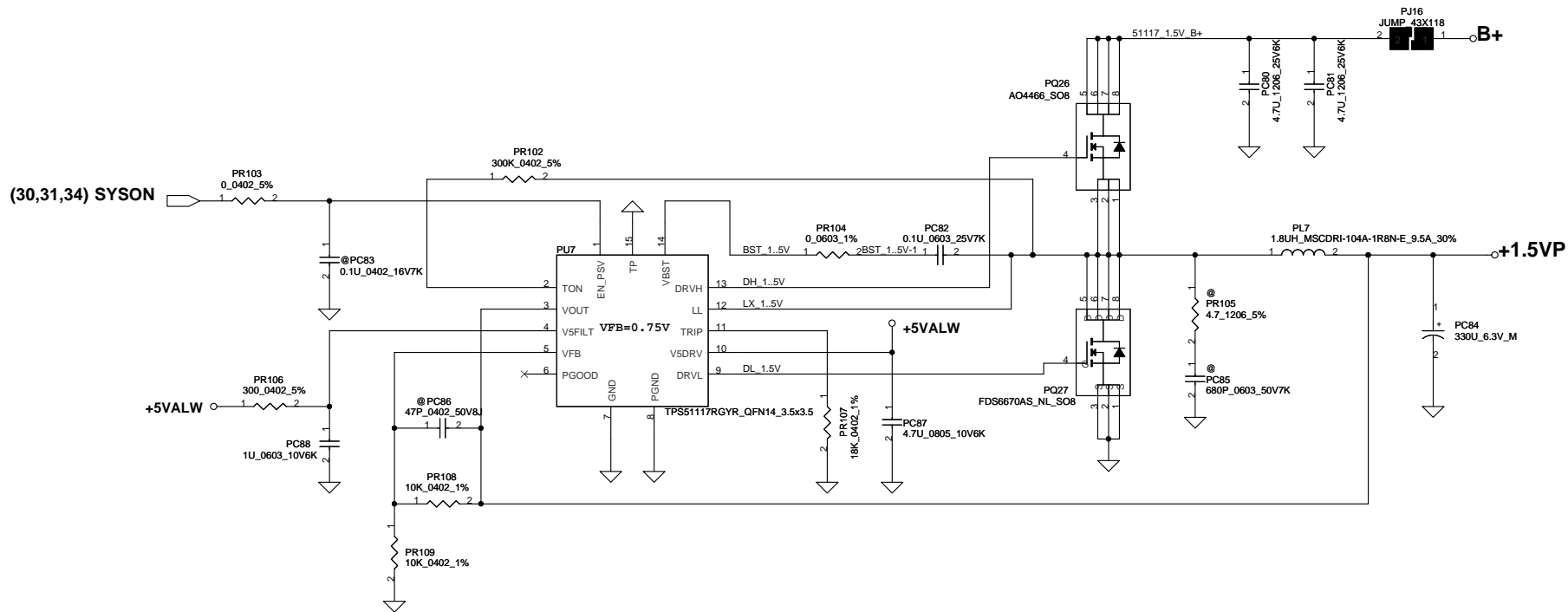
Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	@
4.1V	L	887K	221K
4.2V	H	@	@



VFB=0.75V  
 $V_o = VFB * (1 + PR100 / PR101) = 1.055V$   
 $F_{sw} = 262KHz$

Cout ESR=15m ohm  
 $R_{dsonmax} = 11.5m \text{ ohm}$ ,  $R_{dson typ} = 9m \text{ ohm}$   
 $I_{peak} = 7.15A$ ,  $I_{max} = 3.5A$   
 $\Delta I = ((19 - 1.05) * (1.05 / 19)) / (L * F_{sw}) = 2.103A$   
 $\Rightarrow 1/2 \Delta I = 1.052A$   
 $V_{trip} = R_{trip} * I_{0uA} = 9.09K * 10uA = 0.0909V$   
 $I_{ocpmin} = V_{trip} / R_{dsonmax} * 1.3 + 1.052A = 7.132A$   
 $I_{ocpmax} = V_{trip} / R_{dson typ} * 1.1 + 1.052A = 10.233A$   
 $I_{ocp} = 7.132A - 10.233A$

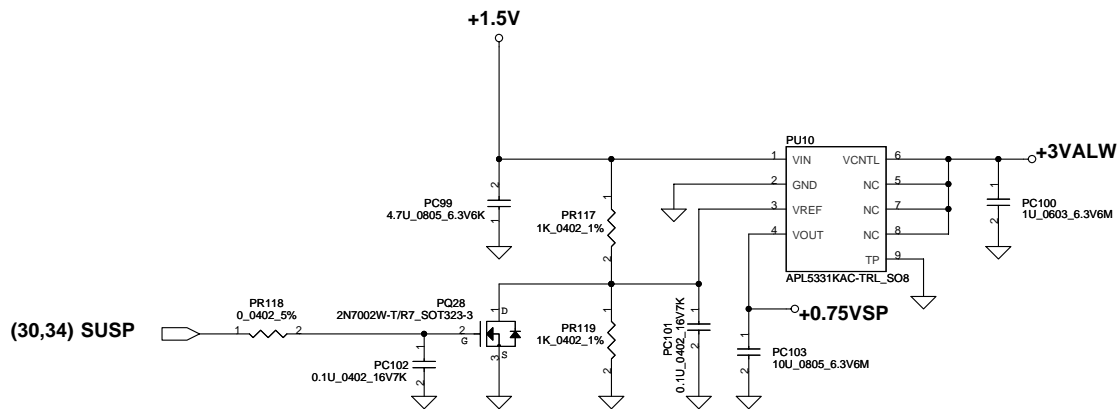
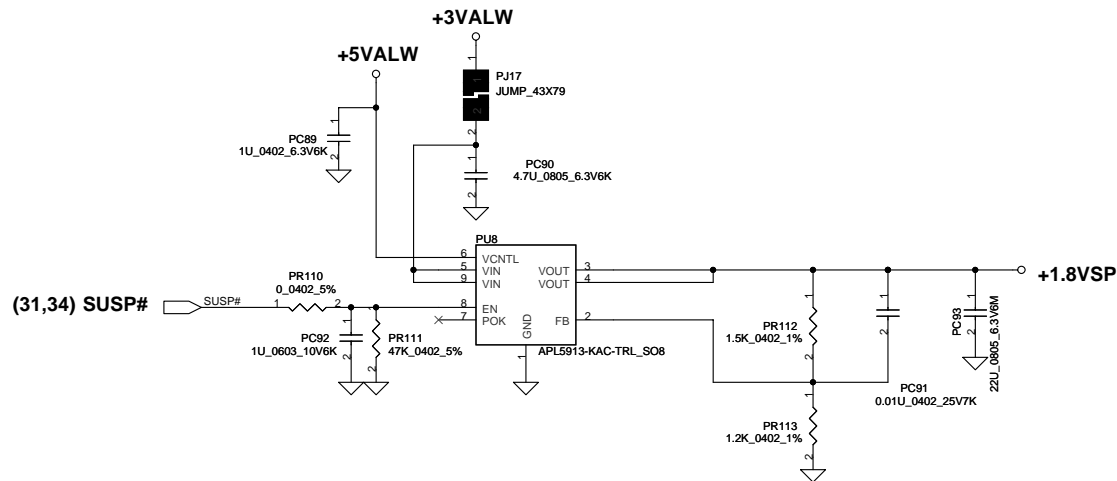
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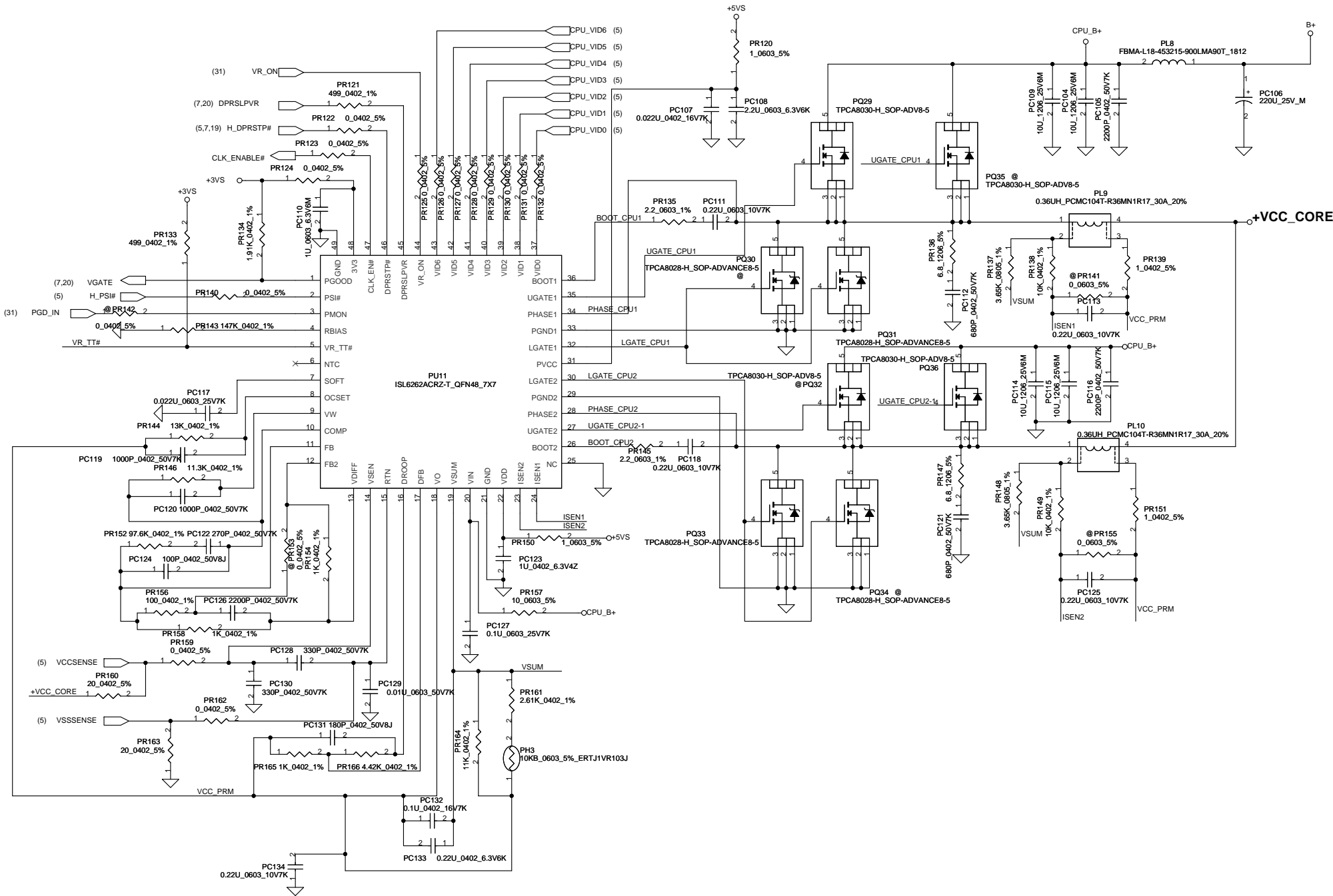
$V_{FB}=0.75V$   
 $V_o=V_{FB}*(1+PR108/PR109)=1.5V$   
 $F_{sw}=262KHz$   
 $C_{out} ESR=15m\ ohm$   
 $R_{dsonmax}=11.5m\ ohm, R_{dson typ}=9m\ ohm$   
 $I_{peak}=13.67A, I_{max}=8A$   
 $\Delta I=((19-1.5)*(1.5/19))/(L*F_{sw})=2.930A$   
 $\Rightarrow 1/2\Delta I=1.465A$   
 $V_{trip}=R_{trip}*I_{max}=18K*10uA=0.180V$   
 $I_{ocpmin}=V_{trip}/R_{dsonmax}*1.4+1.465A=12.645A$   
 $I_{ocpmax}=V_{trip}/R_{dson typ}*1.2+1.465A=18.131A$   
 $I_{ocp}=12.645A-18.131A$

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Solve power noise for HDD signal	Solve power noise for HDD signal	0.1	P37	Change PJ13 to BEAD PL11	12/19	DVT
2	Solve power noise for HDD signal	Solve power noise for HDD signal	0.1	P39	Change PJ15 to BEAD PL12	12/19	DVT
3	+1.05V Efficiency	+1.05V Efficiency	0.1	P39	Change PL6 from 1.2U to 1.0U	12/19	DVT
4	For EMI solution	For EMI solution	0.1	P39	Add PC136,PC137,PC138 ,Change PR96 to 2.2 ohm	12/19	DVT
5	For EMI solution	For EMI solution	0.1	P37	Add PC139	12/19	DVT
6	For EMI solution	For EMI solution	0.1	P42	Change PR135, PR145 to 2.2 ohm	12/19	DVT
7	For EMI solution	For EMI solution	0.2	P39	Pop PR97 and PC76	02/02	PVT
8	Modify CPU MOSFET solution	Modify CPU MOSFET solution	0.2	P42	change PQ29,PQ36 to SB000000HL00	02/02	PVT
9	Modify CPU MOSFET solution	Modify CPU MOSFET solution	0.2	P42	change PQ31,PQ33 to SB000000GL00	02/02	PVT
10	Modify CPU MOSFET solution	Modify CPU MOSFET solution	0.2	P42	Unpop PQ32,PQ35,PQ30,PQ34	02/02	PVT
11	Modify CPU PWM frequency	Modify CPU PWM frequency	0.2	P42	change PR146 to SD034113280	02/02	PVT
12							
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